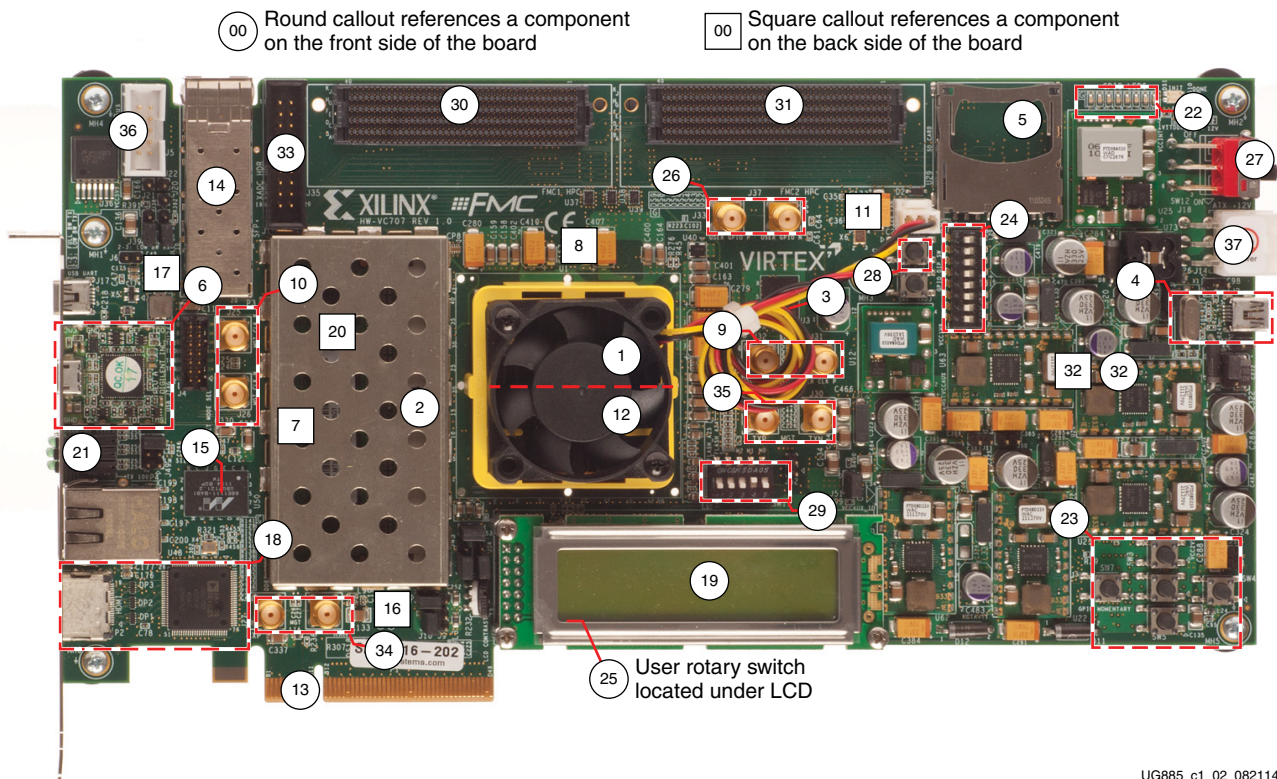


# Feature Descriptions

Figure 1-2 shows the VC707 board. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

**Note:** The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.



UG885\_c1\_02\_082114

Figure 1-2: VC707 Board Component Locations

Table 1-1: VC707 Board Component Descriptions

Callout	Reference Designator	Component Description	Notes	Schematic 0381418 Page Number
1	U1	Virtex-7 FPGA with cooling fan	XC7VX485T-2FFG1761C	
2	J1	DDR3 SODIMM memory (1 GB)	Micron MT8JTF12864HZ-1G6G1	21
3	U3	BPI parallel NOR flash memory (1 Gb)	Micron PC28F00AG18FE	35
4	U8, J2	USB ULPI transceiver, USB mini-B connector	SMSC USB3320-EZK	44
5	U29	SD card interface connector	Molex 67840-8001	37
6	U26	USB JTAG interface, USB micro-B connector	Digilent USB JTAG module	20
7	U51	System clock, 200 MHz, LVDS (back side of board)	SiTime SIT9102-243N25E200.0000	32

Table 1-1: VC707 Board Component Descriptions (Cont'd)

Callout	Reference Designator	Component Description	Notes	Schematic 0381418 Page Number
8	U34	I <sup>2</sup> C programmable user clock LVDS, 156.250 MHz default frequency (back side of board)	Silicon Labs SI570BAB0000544DG	32
9	J31, J32	User SMA clock	Rosenberger 32K10K-400L5	32
10	J25, J26	GTX transceiver SMA reference clock	Rosenberger 32K10K-400L5	32
11	U24	Jitter attenuated clock (back side of board)	Silicon Labs SI5324C-C-GM	33
12		GTX transceiver Quad 111 – Quad 119	Embedded within FPGA U1	12 – 15
13	P1	PCI Express connector	8-lane card edge connector	30
14	P3	SFP/SFP+ module connector	Molex 74441-0010	31
15	U50	10/100/1000 Mb/s Ethernet PHY	Marvell M88E1111-BAB1C000	34
16	U2	SGMII GTX transceiver clock generator	ICS ICS84402IAGI-01LF	32
17	U44	USB-to-UART bridge	Silicon Labs CP2103GM	36
18	P2, U48	HDMI video connector, HDMI controller	Molex 500254-1927, AD ADV7511KSTZ-P	43, 42
19	J23	LCD character display and connector	2 x 7 0.1 inch male header	39
20	U52	I <sup>2</sup> C Bus Switch (back side of board)	TI PCA9548ARGER	41
21	DS11–DS13	Ethernet status LEDs	EPHY status LED, dual green	34
22	DS2–DS9	User LEDs	GPIO LEDs, green 0603	38
23	SW3–SW7	User pushbuttons, active-High	E-Switch TL3301EP100QG	38
24	SW2	User DIP Switch	8-pole C and K SDA08H1SBD	38
25	SW10	User rotary switch (under LCD assembly)	Panasonic EVQ-WK4001	38
26	J33, J34	User SMA GPIO	Rosenberger 32K10K-400L5	32
27	SW12	Power on/off switch	C&K 1201M2S3AQE2	45
28	SW9	FPGA PROG pushbutton	E-Switch TL3301EP100QG	38
29	SW11	Config mode/upper linear flash address dip switch	5-pole C&K SDA05H1IBD	36
30	J35	FMC HPC1 connector (J35)	Samtec ASP_134486_01	22–25
31	J37	FMC HPC2 connector (J37)	Samtec ASP_134486_01	26–29
32		Power management system (front and back side of board)	TI UCD9248PFC in conjunction with various regulators	45–55
33	J19	Xilinx XADC header	2 x 10 0.1inch male header	40
34	J27, J28	GTX receiver SMA (RX)	Rosenberger 32K10K-400L5	32
35	J29/J30	GTX transmitter SMA (TX)	Rosenberger 32K10K-400L5	32
36	J5	2 x 5 shrouded PMBus connector	Assman HW10G-0202	46
37	J18	12V power input 2 x 3 connector	Molex 39-30-1060	46

**Notes:**

1. Jumper header locations are identified in [Appendix A, Default Switch and Jumper Settings](#).

Table 1-13 lists the PCIe edge connector connections for Quad 115.

Table 1-13: GTX Quad 115 PCIe Edge Connector Connections

Quad 115 Pin Name	FPGA (U1) Pin	Net Name	PCIe Edge Connector (P1)		FHG1761 Placement
			Pin	Pin Name	
MGTTXP0_115_AE2	AE2	PCIE_TX3_P	A29	PERp3	GTXE2_CHANNEL_X1Y11
MGTTXN0_115_AE1	AE1	PCIE_TX3_N	A30	PERn3	GTXE2_CHANNEL_X1Y11
MGTXXP0_115_AC6	AC6	PCIE_RX3_P	B27	PETp3	GTXE2_CHANNEL_X1Y11
MGTXXN0_115_AC5	AC5	PCIE_RX3_N	B28	PETn3	GTXE2_CHANNEL_X1Y11
MGTTXP1_115_AC2	AC2	PCIE_TX2_P	A25	PERp2	GTXE2_CHANNEL_X1Y10
MGTTXN1_115_AC1	AC1	PCIE_TX2_N	A26	PERn2	GTXE2_CHANNEL_X1Y10
MGTXXP1_115_AB4	AB4	PCIE_RX2_P	B23	PETp2	GTXE2_CHANNEL_X1Y10
MGTXXN1_115_AB3	AB3	PCIE_RX2_N	B24	PETn2	GTXE2_CHANNEL_X1Y10
MGTTXP2_115_AA2	AA2	PCIE_TX1_P	A21	PERp1	GTXE2_CHANNEL_X1Y9
MGTTXN2_115_AA1	AA1	PCIE_TX1_N	A22	PERn1	GTXE2_CHANNEL_X1Y9
MGTXXP2_115_AA6	AA6	PCIE_RX1_P	B19	PETp1	GTXE2_CHANNEL_X1Y9
MGTXXN2_115_AA5	AA5	PCIE_RX1_N	B20	PETn1	GTXE2_CHANNEL_X1Y9
MGTTXP3_115_W2	W2	PCIE_TX0_P	A16	PERp0	GTXE2_CHANNEL_X1Y8
MGTTXN3_115_W1	W1	PCIE_TX0_N	A17	PERn0	GTXE2_CHANNEL_X1Y8
MGTXXP3_115_Y4	Y4	PCIE_RX0_P	B14	PETp0	GTXE2_CHANNEL_X1Y8
MGTXXN3_115_Y3	Y3	PCIE_RX0_N	B15	PETn0	GTXE2_CHANNEL_X1Y8
MGTREFCLK0P_115_Y8	Y8	NC			MGT_BANK_115
MGTREFCLK0N_115_Y7	Y7	NC			MGT_BANK_115
MGTREFCLK1P_115_AB8	AB8	PCIE_CLK_Q0_P	A13	REFCLK+	MGT_BANK_115
MGTREFCLK1N_115_AB7	AB7	PCIE_CLK_Q0_N	A14	REFCLK-	MGT_BANK_115

Table 1-14 lists the PCIe edge connector connections for Quad 114.

Table 1-14: GTX Quad 114 PCIe Edge Connector Connections

Quad 114 Pin Name	FPGA (U1) Pin	Net Name	PCIe Edge Connector (P1)		FHG1761 Placement
			Pin	PCIe Edge Pin Name	
MGTTXP0_114_AK4	AK4	PCIE_TX7_P	A47	PERp7	GTXE2_CHANNEL_X1Y4
MGTTXN0_114_AK3	AK3	PCIE_TX7_N	A48	PERn7	GTXE2_CHANNEL_X1Y4
MGTXXP0_114_AG6	AG6	PCIE_RX7_P	B45	PETp7	GTXE2_CHANNEL_X1Y4
MGTXXN0_114_AG5	AG5	PCIE_RX7_N	B46	PETn7	GTXE2_CHANNEL_X1Y4
MGTTXP1_114_AJ2	AJ2	PCIE_TX6_P	A43	PERp6	GTXE2_CHANNEL_X1Y5
MGTTXN1_114_AJ1	AJ1	PCIE_TX6_N	A44	PERn6	GTXE2_CHANNEL_X1Y5

Appendix B: VITA 57.1 FMC Connector Pinouts

XC3190TM	2001+	N A	2315
XC3190-PQ208	2001+	QFP	2315
XC3190-PQ160I	2001+	BGA	2315
XC3190PQ160C-4	2001+	QFP	2315
XC3190-PQ160C	2001+	BGA	2315
XC3190PQ160-4	2001+	QFP	2315
XC3190-PQ160	2001+	QFP	2315
XC3190PQ160	2001+	QFP	2315
XC3190PC84C-5	2001+	PLCC	2315
XC3190LTQ176AKJ	2001+	QFP	2315
XC3190LTQ176-2C	2001+	QFP	2315
XC3190LTQ176	2001+	QFP	2315
XC3190LTQ144	2001+	QFP	2315
XC3190LTMPC84C	2001+	PLCC	2315
XC3190LTM	2001+	PLCC	2315
XC3190L-4PC84I	2001+	原厂原封	2315
XC3190L-3TQ176I	2001+	QFP	2315
XC3190L-3TQ176C	2001+	QFP	2315
XC3190L-3TQ144I	2001+	QFP	2315
XC3190L-3TQ144C	2001+	TQFP144	2315
XC3190L-3TQ144C	2001+	TQFP	2315
XC3190L-3PC84C	2001+	BGA	2315
XC3190L-2TQG176C	2001+	TQFP-176	2315
XC3190L-2TQG144C	2001+	QFP	2315
XC3190L-2TQ176I	2001+	QFP	2315
XC3190L-2TQ176C	2001+	BGA	2315
XC3190L-2TQ144I	2001+	QFP	2315
XC3190L-2TQ144C	2001+	BGA	2315
XC3190L-2PC84C	2001+	BGA	2315
XC3190L-1TQ144C	2001+	QFP	2315
XC3190L	2001+	BGA	2315
XC3190ATQ176-5	2001+	TQFP	2315
XC3190ATQ176	2001+	TQFP	2315
XC3190ATQ144	2001+	TQFP	2315
XC3190ATM-PQ160-3C	2001+	QFP	2315
XC3190ATMPQ160-3	2001+	QFP	2315
XC3190ATM-5PQ160C	2001+	QFP	2315
XC3190ATM-5PG175BFQG	2001+	PGA	2315
XC3190ATM-5PC84I	2001+	PLCC84	2315
XC3190ATM-5PC84C	2001+	PLCC	2315
XC3190ATM-5	2001+	N A	2315

Appendix C: Xilinx Constraints File

XC3190ATM/3C	2001+	PLCC84	2315
XC3190ATM PC84	2001+	PLCC84	2315
XC3190ATM	2001+	QFP	2315
XC3190A-PQG1600AKJ	2001+	QFP	2315
XC3190APQ208-5	2001+	QFP	2315
XC3190APQ208-4C	2001+	QFP	2315
XC3190APQ208-3C	2001+	QFP	2315
XC3190APQ208	2001+	QFP	2315
XC3190APQ160AKJ3C	2001+	QFP	2315
XC3190A-PQ160AKJ	2001+	PQFP	2315
XC3190A-PQ160AK	2001+	QFP	2315
XC3190A-PQ160A	2001+	QFP	2315
XC3190A-PQ160-5C	2001+	QFP	2315
XC3190APQ160-5C	2001+	QFP	2315
XC3190A-PQ160-4C	2001+	QFP	2315
XC3190APQ160-4C	2001+	QFP	2315
XC3190APQ160-3C	2001+	QFP	2315
XC3190APQ160-3	2001+	QFP	2315
XC3190APQ160-2C	2001+	QFP	2315
XC3190A-PQ160	2001+	QFP	2315
XC3190APQ160	2001+	QFP	2315
XC3190A-PG175AKJ	2001+	PGA	2315
XC3190A-PC84CKG	2001+	PGA	2315
XC3190APC84-5I	2001+	PLCC84	2315
XC3190APC84-5C	2001+	PLCC84	2315
XC3190APC84-4I	2001+	PLCC84	2315
XC3190APC84-4C	2001+	PLCC84	2315
XC3190APC84-3C	2001+	PLCC84	2315
XC3190APC84-3	2001+	PLCC	2315
XC3190APC84	2001+	PLCC84	2315
XC3190A-9TQ176C	2001+	BGA	2315
XC3190A-7PQG160C	2001+	QFP	2315
XC3190A-7PQ208C	2001+	QFP	2315
XC3190A-7PQ160C	2001+	QFP	2315
XC3190A-6TQ176C	2001+	QFP	2315
XC3190A-6PQ208	2001+	QFP	2315
XC3190A-6PQ160	2001+	QFP	2315
XC3190A-5TQG176I	2001+	QFP	2315
XC3190A-5TQ176C	2001+	TQFP	2315
XC3190A-5PQG208I	2001+	QFP208	2315
XC3190A-5PQG208C	2001+	QFP208	2315