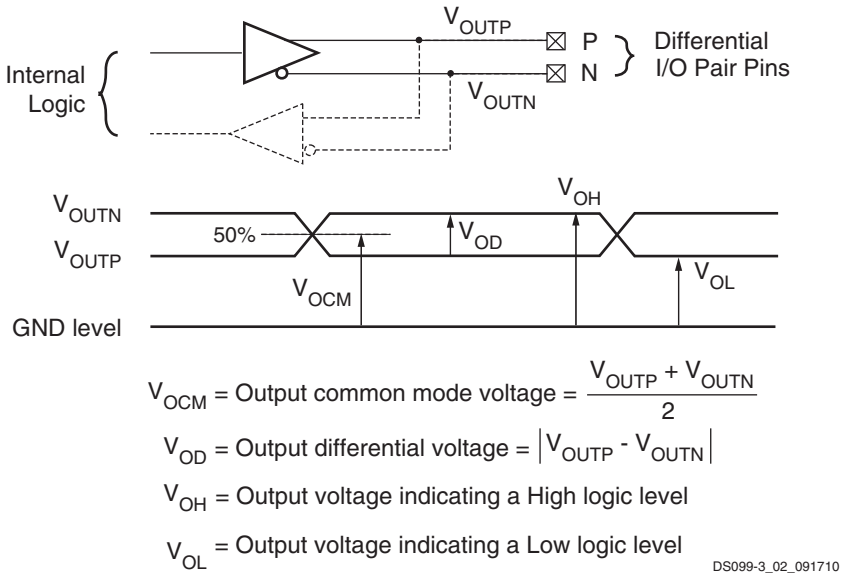


Figure 33: **Differential Output Voltages**

Table 38: **DC Characteristics of User I/Os Using Differential Signal Standards**

Signal Standard	Mask[3] Revision	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
		Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LDT_25 (ULVDS_25)	All	430[4]	600	670	0.495	0.600	0.715	0.71	0.50
LVDS_25	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	200	–	500	1.0	–	1.5	1.10	1.40
BLVDS_25[5]	All	250	350	450	–	1.20	–	–	–
LVDSEXT_25	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	300	–	700	1.0	–	1.5	1.15	1.35
LVPECL_25[5]	All	–	–	-	–	–	-	1.35	1.005
RSDS_25[6]	All	100	–	600	0.80	–	1.6	0.85	1.55
	'E'	200	–	500	1.0	–	1.5	1.10	1.40
DIFF_HSTL_II_18	All	–	–	–	–	–	–	V_{CCO} – 0.40	0.40
DIFF_SSTL2_II	All	–	–	–	–	–	–	V_{TT} + 0.80	V_{TT} – 0.80

Notes:

1. The numbers in this table are based on the conditions set forth in Table 32 and Table 37.
2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
3. Mask revision E devices have tighter output ranges but can be used in any design that was in a previous revision. See Mask and Fab Revisions, page 58.
4. This value must be compatible with the receiver to which the FPGA's output pair is connected.
5. Each LVPECL_25 or BLVDS_25 output-pair requires three external resistors for proper output operation as shown in Figure 34. Each LVPECL_25 or BLVDS_25 input-pair uses a 100W termination resistor at the receiver.
6. Only one of the differential standards RSDS_25, LDT_25, LVDS_25, and LVDSEXT_25 may be used for outputs within a bank. Each differential standard input-pair requires an external 100Ω termination resistor.

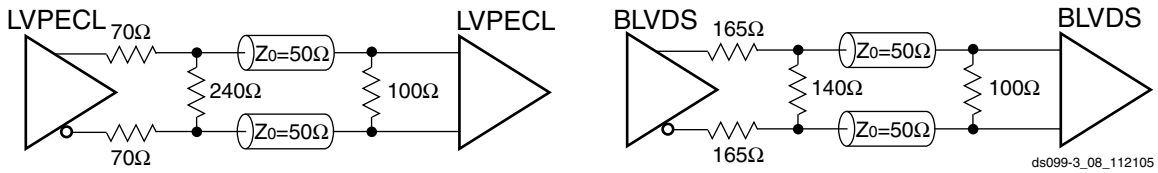


Figure 34: **External Termination Required for LVPECL and BLVDS Output and Input**

XC3164-4PQ160I	2001+	QFP160	2315
XC3164-4PQ160C	2001+	NA	2315
XC3164-4PC84I	2001+	BGA	2315
XC3164-4PC84C	2001+	BGA	2315
XC3164-4C/TQ144	2001+	QFP	2315
XC3164-3PQ160I	2001+	QFP160	2315
XC3164-3PQ160C	2001+	QFP	2315
XC3164-3PC84I	2001+	PLCC	2315
XC3164-3PC84C	2001+	PLCC	2315
XC3164-3PC84	2001+	PLCC	2315
XC3164-2PQ160C	2001+	原厂原封	2315
XC3164-2PC84I	2001+	PLCC	2315
XC3164-2PC84C	2001+	PLCC	2315
XC3164-1PC84C	2001+	PLCC	2315
XC3164-125PQ160C	2001+	BGA	2315
XC3164-100	2001+	PLCC	2315
XC31500-4FG676C	2001+	BGA	2315
XC3146ATQ144	2001+	QFP	2315
XC3146A-4PQ160C	2001+	QFP-160	2315
XC3146A-3PQ160C	2001+	QFP-160	2315
XC3146A-1PQ160I	2001+	QFP-160	2315
XC3142VQ100	2001+	TQFP	2315
XC3142TQ144-3C	2001+	TQFP	2315
XC3142TQ100	2001+	TQFP	2315
XC3142TM-5PC84	2001+	PLCC	2315
XC3142TM-4-PC84C	2001+	PLCC84	2315
XC3142TM-4PC84C	2001+	PLCC	2315
XC3142TM-4PC84	2001+	PLCC	2315
XC3142TM-3PC84C	2001+	PLCC84	2315
XC3142TM-3PC84	2001+	PLCC	2315
XC3142QC160-3	2001+	BGA	2315
XC3142PQ100-5	2001+	QFP	2315
XC3142PQ100-3	2001+	QFP	2315
XC3142PQ100	2001+	QFP	2315
XC3142PM-3PC84	2001+	PLCC	2315
XC3142PC84	2001+	PLCC	2315
XC3142MPQ100	2001+	QFP	2315
XC3142LVQ100	2001+	QFP	2315
XC3142L-3VQG100C	2001+	QFP	2315
XC3142L-3VQ160C	2001+	BGA	2315
XC3142L-3VQ100I	2001+	QFP	2315

Switching Characteristics

All Spartan-3 devices are available in two speed grades: –4 and the higher performance –5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reported delays may still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Production-quality systems must use FPGA designs compiled using a Production status speed file. FPGAs designs using a less mature speed file designation may only be used during system prototyping or preproduction qualification. FPGA designs using Advance or Preliminary status speed files should never be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All specified limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the following applies: Parameter values apply to all Spartan-3 devices. All parameters representing voltages are measured with respect to GND.

Selected timing parameters and their representative values are included below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3 FPGA v1.38 speed files are the original source for many but not all of the values. The v1.38 speed files are available in Xilinx Integrated Software Environment (ISE) software version 8.2i.

The speed grade designations for these files are shown in Table 39. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 39: **Spartan-3 FPGA Speed Grade Designations (ISE v8.2i or Later)**

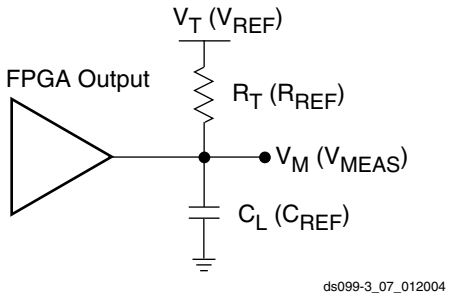
Device	Advance	Preliminary	Production
XC3S50			-4, -5 (v1.37 and later)
XC3S200			
XC3S400			
XC3S1000			
XC3S1500			
XC3S2000			
XC3S4000			
XC3S5000			-4, -5 (v1.38 and later)

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 48 presents the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 35. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (e.g., LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 35: **Output Test Setup**

Table 48: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended						
GTL	0.8	V_{REF} – 0.2	V_{REF} + 0.2	25	1.2	V_{REF}
GTL_DCI				50	1.2	
GTLP	1.0	V_{REF} – 0.2	V_{REF} + 0.2	25	1.5	V_{REF}
GTLP_DCI				50	1.5	
HSLVDCI_15	0.9	V_{REF} – 0.5	V_{REF} + 0.5	1M	0	0.75
HSLVDCI_18						0.90
HSLVDCI_25						1.25
HSLVDCI_33						1.65
HSTL_I	0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_I_DCI						
HSTL_III	0.90	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_III_DCI						
HSTL_I_18	0.90	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_I_DCI_18						
HSTL_II_18	0.90	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_DCI_18						

XC3142A-VQ100-4C	2001+	QFP	2315
XC3142A-VQ100	2001+	QFP	2315
XC3142AVQ100	2001+	QFP	2315
XC3142ATQ144-5C	2001+	QFP	2315
XC3142ATQ144-4C	2001+	QFP	2315
XC3142ATQ144-3C	2001+	QFP	2315
XC3142ATQ144-2C	2001+	QFP	2315
XC3142ATQ144	2001+	QFP	2315
XC3142ATQ100	2001+	QFP	2315
XC3142ATMPQ100	2001+	QFP	2315
XC3142ATMPC84	2001+	PLCC	2315
XC3142ATM-5PC842	2001+	PLCC	2315
XC3142ATM-5PC84	2001+	PLCC	2315
XC3142ATM-5	2001+	PLCC	2315
XC3142ATM-4PC84C	2001+	PLCC	2315
XC3142ATM-4PC84	2001+	PLCC84	2315
XC3142ATM-3PC84	2001+	PLCC	2315
XC3142ATM-3 PQ100C	2001+	QFP	2315
XC3142ATM-3	2001+	N A	2315
XC3142ATM	2001+	BGA	2315
XC3142ATA144	2001+	QFP	2315
XC3142AQ100	2001+	QFP	2315
XC3142A-PQ100AKJ	2001+	QFP100	2315
XC3142APQ100-7I	2001+	QFP	2315
XC3142APQ100-5C	2001+	QFP	2315
XC3142APQ100-4C	2001+	QFP	2315
XC3142APQ100-3C	2001+	QFP	2315
XC3142A-PQ100	2001+	QFP	2315
XC3142APQ100	2001+	QFP	2315
XC3142APG84DKG-3C	2001+	PGA84	2315
XC3142APG132DKG	2001+	BGA	2315
XC3142APC84AKJ0021	2001+	PLCC84	2315
XC3142A-PC84AKJ	2001+	PLCC-84	2315
XC3142APC84-5	2001+	PLCC	2315
XC3142APC84-4C	2001+	PLCC84	2315
XC3142APC84-4+	2001+	PLCC	2315
XC3142APC84-4	2001+	PLCC	2315
XC3142APC84-3C	2001+	PLCC	2315
XC3142APC84-3	2001+	PLCC	2315
XC3142A-PC84	2001+	PLCC	2315
XC3142A-9PQ100C	2001+	QFP	2315