Chapter 6

Configuration Details

Configuration Memory Frames

Virtex®-5 FPGA configuration memory is arranged in frames that are tiled about the device. These frames are the smallest addressable segments of the Virtex-5 configuration memory space, and all operations must therefore act upon whole configuration frames. Virtex-5 frame counts and configuration sizes are shown in Table 6-1. Depending on BitGen options, additional overhead exists in the configuration bitstream. The exact bitstream length is available in the rawbits file (.rbt) created by using the "-b" option with bitgen or selecting "Create ASCII Configuration File" in the Generate Programming File options popup in ISE. Bitstream length (words) are roughly equal to the configuration array size (words) plus configuration overhead (words). Bitstream length (bits) are roughly equal to the bitstream length in words times 32.

Table 6-1: **Virtex-5 Device Frame Count, Frame Length, Overhead, and Bitstream Size**

Device	Non-Configuration Frames(1)	Configuration Frames	Total Device Frames	Frame Lengths in Words(2)	Configuration Array Size in Words(3)	Bitstream Overhead in Words(4)
LX30	172	6,376	6,548	41	261,416	272
LX50	258	9,564	9,822	41	392,124	272
LX85	426	16,644	17,070	41	682,404	272
LX110	568	22,192	22,760	41	909,872	272
LX155	800	32,544	33,344	41	1,334,304	272
LX220	1,040	40,496	41,536	41	1,660,336	272
LX330	1,560	60,744	62,304	41	2,490,504	272
LX20T	126	3,762	3,888	41	154,242	272
LX30T	184	7,136	7,320	41	292,576	272
LX50T	276	10,704	10,980	41	438,864	272
LX85T	444	17,784	18,228	41	729,144	272
LX110T	592	23,712	24,304	41	972,192	272
LX155T	808	32,800	33,608	41	1,344,800	272
LX220T	1,064	42,016	43,080	41	1,722,656	272
LX330T	1,596	63,024	64,620	41	2,583,984	272
SX35T	244	10,168	10,412	41	416,888	272
SX50T	366	15,252	15,618	41	625,332	272

XC3142A-5TQG144C	2001+	QFP	2315
XC3142A-5TQ144I	2001+	QFP	2315
XC3142A-5TQ144C	2001+	BGA	2315
XC3142A-5TQ100C	2001+	QFP	2315
XC3142A-5PQ100I	2001+	BGA	2315
XC3142A-5PQ100C	2001+	QFP	2315
XC3142A5PQ100C	2001+	QFP	2315
XC3142A-5PG84M	2001+	原厂原封	2315
XC3142A-5PG84I	2001+	PGA	2315
XC3142A-5PG84C	2001+	PGA	2315
XC3142A-5PG84B	2001+	PGA	2315
XC3142A-5PG132I	2001+	PGA	2315
XC3142A-5PG132C	2001+	PGA	2315
XC3142A-5PG132B	2001+	PGA	2315
XC3142A-5PC84I	2001+	PLCC84	2315
XC3142A-5PC84C	2001+	PLCC-84	2315
XC3142A-5PC84	2001+	PLCC	2315
XC3142A-5CB100B	2001+	PGA	2315
XC3142A-5	2001+	QFP	2315
XC3142A-4VQG100I	2001+	QFP	2315
XC3142A-4VQG100C	2001+	QFP	2315
XC3142A-4VQ100I	2001+	TQFP100	2315
XC3142A-4VQ100C	2001+	QFP100	2315
XC3142A-4VQ100	2001+	QFP	2315
XC3142A-4TQG100C	2001+	QFP	2315
XC3142A-4TQ144I	2001+	BGA	2315
XC3142A-4TQ144C	2001+	TQFP144	2315
XC3142A-4TQ100I	2001+	QFP	2315
XC3142A-4TQ100C	2001+	QFP	2315
XC3142A-4TI144I	2001+	NA	2315
XC3142A-4PQG100C	2001+	QFP	2315
XC3142A-4PQ84C	2001+	原厂原封	2315
XC3142A-4PQ100I	2001+	QFP	2315
XC3142A-4PQ100C	2001+	QFP100	2315
XC3142A-4PP132C	2001+	PGBA	2315
XC3142A-4PG84M	2001+	NA	2315
XC3142A-4PG84I	2001+	PGA	2315
XC3142A-4PG84C	2001+	PGA	2315
XC3142A-4PG84B	2001+	PGA	2315
XC3142A-4PG132I	2001+	PGA	2315
XC3142A-4PG132C	2001+	PGA	2315

The syndrome bits S[10:0] are derived from the Hamming parity bits, while S[11] is derived from the overall parity bit. The syndrome bit is interpreted as follows:

`S[11] = 0, S[10:0] = 0:` no error.

`S[11] = 1, S[10:0] ≠ 0:` single bit (SED) error; S[10:0] denotes location of bit to patch (indirectly).

`S[11] = 1, S[10:0] = 0:` single-bit error; overall parity bit p[11] is in error.

`S[11] = 0, S[10:0] ≠ 0:` double-bit error, not correctable.

In case of a single-bit error in the frame data, the syndrome bits S[10:0] points to the flipped bit in the address space from 704 (location of the first bit in the frame) to 2047 (last bit in the frame). To convert the syndrome value S[10:0] to the index of the flipped bit in the range 0 to 1311, subtract 704 decimal (`2C0` hexadecimal or `01011000000` binary) if the syndrome is less than 1,024 decimal; otherwise, subtract 736 decimal (`2E0` hexadecimal or `01011100000` binary). This is equivalent to subtracting 22 or 23 decimal from S[10:5], and can be calculated as `bit_index = {S[10:5] -6'd22-S[10],S[5:0]}`.

If S[10:0] is `0` or a power of 2, however, an error in a parity bit has occurred. The Hamming parity bits are stored in locations 640–651. If bit S[11] indicates a single-bit error, then (in the case of a Hamming code parity bit error) a `1` is presented in the appropriate power-of-2 bit position, with the other syndrome bits set to `0`:

```
100000000001 ->  640
100000000010 ->  641
100000000100 ->  642
100000001000 ->  643
100000010000 ->  644
100000100000 ->  645
100001000000 ->  646
100010000000 ->  647
100100000000 ->  648
101000000000 ->  649
110000000000 ->  650
100000000000 ->  651
```

Table 4-4 defines the FRAME_ECC_VIRTEX5 pins. See Chapter 9, "Readback CRC" for more information.

Table 4-4: **FRAME_ECC_VIRTEX5 Pin Table**

Pin Name	Type	Description
SYNDROMEVALID	Output	Frame ECC syndrome valid pulse. Active one cycle for each frame. Used to sample ERROR and SYNDROME[11:0].
ECCERROR	Output	When SYNDROMEVALID is active, this output signals if a frame error was detected or not. • ERROR = 1 when SYNDROME[11:0] is non-zero. • ERROR = 0 when SYNDROME[11:0] is all zeros.

XC3142A-3VQG100I	2001+	QFP	2315
XC3142A-3VQG100C	2001+	QFP	2315
XC3142A-3VQ100I	2001+	QFP	2315
XC3142A-3VQ100C	2001+	QFP100	2315
XC3142A-3VQ100	2001+	QFP	2315
XC3142A-3TQG144I	2001+	QFP	2315
XC3142A-3TQG144C	2001+	QFP	2315
XC3142A-3TQ144I	2001+	TQFP144	2315
XC3142A-3TQ144C	2001+	QFP	2315
XC3142A-3TQ100C	2001+	QFP100	2315
XC3142A-3TI144C	2001+	NA	2315
xc3142a-3pqg100c	2001+	QFP	2315
XC3142A-3PQ100I	2001+	TQFP	2315
XC3142A-3PQ100C	2001+	QFP100	2315
XC3142A3PQ100C	2001+	BGA	2315
XC3142A-3PQ100	2001+	QFP	2315
XC3142A-3PP132C	2001+	PGA	2315
XC3142A-3PCG84I	2001+	PLCC-84	2315
XC3142A-3PCG84C	2001+	PLCC-84	2315
XC3142A-3PC84I	2001+	NA	2315
XC3142A-3PC-84C	2001+	PLCC	2315
XC3142A-3PC84C	2001+	PLCC84	2315
XC3142A-3PC84	2001+	PLCC	2315
XC3142A-3PC8	2001+	BGA	2315
XC3142A-3PC100C	2001+	QFP100	2315
XC3142A-2VQ100I	2001+	BGA	2315
XC3142A-2VQ100C	2001+	BGA	2315
XC3142A-2TQG144I	2001+	QFP	2315
XC3142A-2TQG144C	2001+	QFP	2315
XC3142A-2TQ144I	2001+	BGA	2315
XC3142A-2TQ144C	2001+	BGA	2315
XC3142A-2PQG100I	2001+	TQFP	2315
XC3142A-2PQG100C	2001+	QFP-100	2315
XC3142A-2PQ144C	2001+	QFP	2315
XC3142A-2PQ100I	2001+	LQFP100	2315
XC3142A-2PQ100C	2001+	QFP100	2315
XC3142A-2PQ100	2001+	QFP	2315
XC3142A-2PI100C	2001+	NA	2315
XC3142A-2PCG84C	2001+	PLCC-84	2315
XC3142A-2PC84I	2001+	PLCC	2315
XC3142A-2PC84C	2001+	QFP	2315

Table 6-1: **Virtex-5 Device Frame Count, Frame Length, Overhead, and Bitstream Size *(Continued)***

Device	Non-Configuration Frames(1)	Configuration Frames	Total Device Frames	Frame Lengths in Words(2)	Configuration Array Size in Words(3)	Bitstream Overhead in Words(4)
SX95T	648	27,216	27,864	41	1,115,856	272
SX240T	1,440	60,672	62,112	41	2,487,552	272
FX30T	244	10,296	10,540	41	422,136	272
FX70T	488	20,592	21,080	41	844,272	272
FX100T	696	30,016	30,712	41	1,230,656	272
FX130T	870	37,520	38,390	41	1,538,320	272
FX200T	1,236	54,000	55,236	41	2,214,000	272
TX150T	810	32,980	33,790	41	1,352,180	272
TX240T	1,236	50,112	51,348	41	2,054,592	272

1. Non-configuration frames do not contribute to the bitstream size.
2. All Virtex-5 configuration frames consist of 41 32-bit words.
3. Configuration array size equals the number of configuration frames times the number of words per frame.
4. Configuration overhead consists of commands in the bitstream that are needed to perform configuration but do not themselves program any memory cells. Configuration overhead contributes to the overall bitstream size.

Configuration Registers

All Virtex-5 FPGA bitstream commands are executed by reading or writing to the configuration registers.

Packet Types

The FPGA bitstream consists of two packet types: Type 1 and Type 2. These packet types and their usage are described below.

Type 1 Packet

The Type 1 packet is used for register reads and writes. Only 5 out of 14 register address bits are used in Virtex-5 FPGAs. The header section is always a 32-bit word.

Following the Type 1 packet header is the Type 1 Data section, which contains the number of 32-bit words specified by the word count portion of the header.

Table 6-2: **Type 1 Packet Header Format**

Header Type	Opcode	Register Address	Reserved	Word Count
[31:29]	[28:27]	[26:13]	[12:11]	[10:0]
001	xx	RRRRRRRRRxxxxx	RR	xxxxxxxxxxx

Notes:

1. "R" means the bit is not used and reserved for future use.