Power-On Sequence Precautions

At power-on, the FPGA automatically starts its configuration procedure. When the FPGA is in a Master-BPI configuration mode, the FPGA asserts FCS_B Low and drives a sequence of addresses to read the bitstream from a BPI Flash. The BPI Flash must be ready for asynchronous reads before the FPGA drives FCS_B Low and outputs the first address to ensure the BPI Flash can output the stored bitstream.

Because different power rails can supply the FPGA and BPI Flash or because the FPGA and BPI flash can respond at different times along the ramp of a shared power supply, special attention to the FPGA and BPI Flash power-on sequence or power-on ramps is essential. The power-on sequence or power supply ramps can cause the FPGA to awake before the BPI Flash or vice versa. For many systems with near-simultaneous power supply ramps, the FPGA power-on reset time (TPOR) can sufficiently delay the start of the FPGA configuration procedure such that the BPI Flash becomes ready before the start of the FPGA configuration procedure. In general, the system design must consider the effect of the power sequence, the power ramps, FPGA power-on reset time, and BPI Flash power-on reset time on the timing relation between the start of FPGA configuration and the readiness of the BPI Flash for asynchronous reads. Check DS202, *Virtex-5 FPGA Data Sheet: DC and Switching Characteristics* data sheet for Virtex-5 FPGA power supply requirements and timing. Check DS617, *Platform Flash XL High-Density Configuration and Storage Device* data sheet for the BPI Flash power supply requirements and timing.

One of the following system design approaches can ensure that the BPI Flash is ready for asynchronous reads before the FPGA starts its configuration procedure:

- Control the sequence of the power supplies such that the BPI Flash is certain to be powered and ready for asynchronous reads before the FPGA begins its configuration procedure.
- Hold the FPGA PROGRAM_B pin Low from power-up to delay the start of the FPGA configuration procedure and release the PROGRAM_B pin to High after the BPI flash is fully powered and is able to perform asynchronous reads.
- Hold the FPGA INIT_B pin Low from power-up to delay the start of the FPGA configuration procedure and release the INIT_B pin to High after the BPI flash becomes ready for asynchronous reads.

See the *Power-On Precautions if 3.3V Supply is Last in Sequence* subsection of the Master BPI Mode section in UG332, *Spartan-3 Generation Configuration User Guide*, for reference.

Page Mode Support

Many NOR Flash devices support asynchronous page reads. The first access to a page usually takes the longest time (~100 ns), subsequent accesses to the same page take less time (~25 ns). The following parameters are bitstream programmable in Virtex-5 devices to take advantage of page reads and maximize the CCLK frequency:

- Page sizes of 1 (default), 4, or 8.

  If the actual Flash page size is larger then 8, the value of 8 should be used to maximize the efficiency.
- First access CCLK cycles of 1 (default), 2, 3, or 4. CCLK cycles must be 1 if the page size is 1.
- CCLK frequency

The sequence of page-mode operation is controlled by the Virtex-5 bitstream (see Table 6-15). After an FPGA reset, the default page size is 1, the first access CCLK is 1, and

XC3190A-1PC84C	2001+	BGA	2315
XC3190A-1CTQ176	2001+	原厂原封	2315
XC3190A-1C/PQ160	2001+	QFP	2315
XC3190A-10PQ160C	2001+	QFP-160	2315
XC3190A-09TQG176I	2001+	QFP	2315
XC3190A-09TQ176C	2001+	QFP	2315
XC3190A-09TQ144C	2001+	NA	2315
XC3190A-09PQG160I	2001+	QFP	2315
XC3190A-09PQG160C	2001+	QFP	2315
XC3190A-09PQ208I	2001+	QFP	2315
XC3190A-09PQ208C	2001+	BGA	2315
XC3190A-09PQ160I	2001+	QFP160	2315
XC3190A-09PQ160C	2001+	QFP	2315
XC3190A-09PP175C	2001+	BGA	2315
XC3190A-09PG175C	2001+	BGA	2315
XC3190A-09PC84C	2001+	QFP	2315
XC3190A(TM)-3PQ160C	2001+	QFP	2315
XC3190A PQ160CIG	2001+	QFP	2315
XC3190A PC84	2001+	PLCC	2315
XC3190A 3PQ160C	2001+	QFP	2315
XC3190A PQ160	2001+	QFP	2315
XC3190A	2001+	BGA	2315
XC3190-7TQ176C	2001+	QFP	2315
XC3190-5PQG160I	2001+	QFP	2315
XC3190-5PQ208I	2001+	BGA	2315
XC3190-5PQ208C	2001+	BGA	2315
XC3190-5PQ160I	2001+	BGA	2315
XC3190-5PQ160C	2001+	QFP160	2315
XC3190-5PG175I	2001+	PGA	2315
XC3190-5PC84I	2001+	BGA	2315
XC3190-5PC84C	2001+	BGA	2315
XC31905PC84C	2001+	BGA	2315
XC3190-5 PQ208C	2001+	QFP	2315
XC3190-4PQ208C	2001+	BGAQFP	2315
XC3190-4PQ160I	2001+	QFP160	2315
XC3190-4PQ160C	2001+	BGA	2315
XC31904PQ160C	2001+	BGA	2315
XC3190-4PG175I	2001+	PGA175	2315
XC3190-4PG175C	2001+	原厂原封	2315
XC3190-4PC84I	2001+	PLCC	2315
XC3190-3PQ208I	2001+	QFP208	2315

XC3190-3PG175C	2001+	PGA	2315
XC3190-3PC84C	2001+	BGA	2315
XC3190-3APQ160C	2001+	QFP160	2315
XC3190-2TQG176C	2001+	QFP	2315
XC3190-2TQ176I	2001+	QFP	2315
XC3190-2TQ176C	2001+	QFP	2315
XC31901L-2TQ144C	2001+	原厂原封	2315
XC3190 A-6TQ176C	2001+	QFP	2315
XC3190 4PC84C	2001+	BGA	2315
XC3190	2001+	PLCC	2315
XC3164-TQ144	2001+	QFP	2315
XC3164TQ144	2001+	QFP	2315
XC3164TM-5PC84	2001+	PLCC	2315
XC3164TM-5	2001+	PLCC	2315
XC3164-PQ160-3C	2001+	QFP	2315
XC3164PQ160	2001+	QFP	2315
XC3164ATQ144C	2001+	QFP	2315
XC3164A-TQ144AKJ	2001+	TQFP	2315
XC3164ATQ144-3C	2001+	TQFP	2315
XC3164ATQ144 3C	2001+	QFP	2315
XC3164A-TQ144	2001+	QFP	2315
XC3164ATM-PC84AKJ	2001+	PLCC84	2315
XC3164ATM-5	2001+	PLCC-84	2315
XC3164ATM-4PC84	2001+	PLCC84	2315
XC3164ATM-3PC84C	2001+	PLCC	2315
XC3164ATM-3PC84	2001+	PLCC	2315
XC3164Atm	2001+	PLCC	2315
XC3164A-PQ160C	2001+	BGA	2315
XC3164APQ160AKJ-4C	2001+	QFP	2315
XC3164A-PQ160AKJ	2001+	QFP	2315
XC3164APQ160-5C	2001+	QFP	2315
XC3164APQ160-5	2001+	QFP	2315
XC3164A-PQ160-4C	2001+	QFP	2315
XC3164A-PQ160-3C	2001+	QFP	2315
XC3164A-PQ160	2001+	QFP	2315
XC3164APQ160	2001+	QFP	2315
XC3164APG132CK	2001+	PGA	2315
XC3164APC84C5	2001+	BGA	2315
XC3164APC84-4	2001+	PLCC	2315
XC3164APC84-3	2001+	PLCC	2315
XC3164A-PC84	2001+	PLCC	2315

Capture-DR:
In this controller state, the data is parallel-loaded into the data registers selected by the current instruction on the rising edge of TCK.

Shift-Dr, Exit1-DR, Pause-DR, Exit2-DR, and Update-DR:
These controller states are similar to the Shift-IR, Exit1-IR, Pause-IR, Exit2-IR, and Update-IR states in the Instruction path.

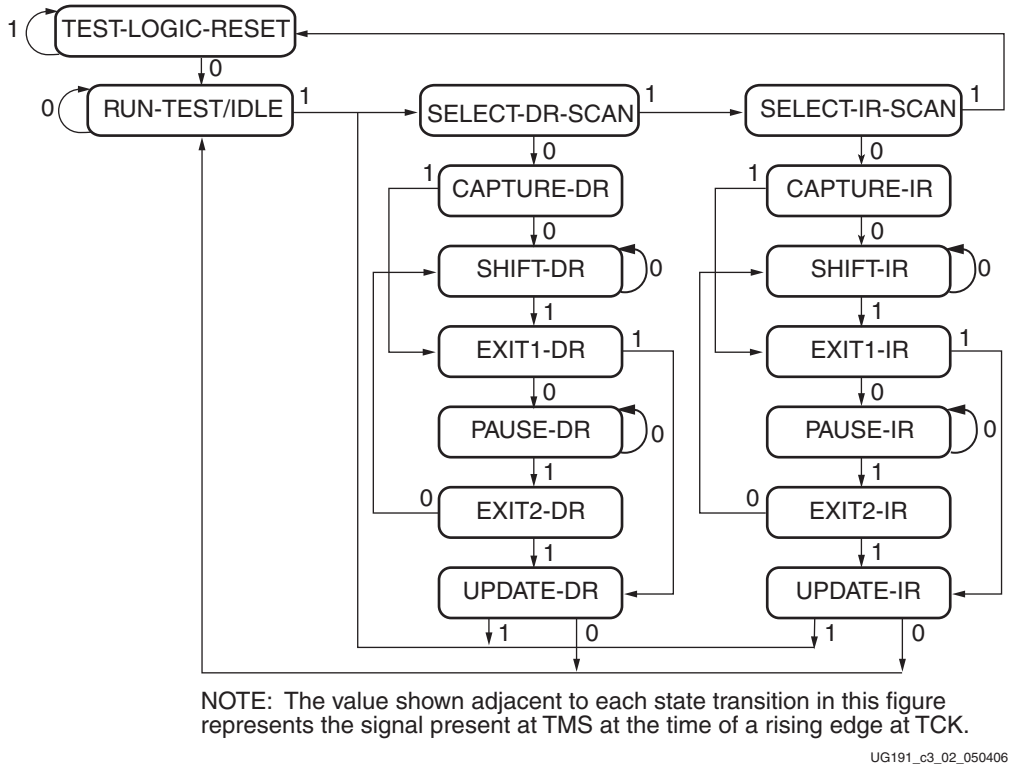

Figure 3-2: **Boundary-Scan TAP Controller**

Virtex-5 devices support the mandatory IEEE 1149.1 commands, as well as several Xilinx vendor-specific commands. The EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions are all included. The TAP also supports internal user-defined registers (USER1, USER2, USER3, and USER4) and configuration/readback of the device.

The Virtex-5 Boundary-Scan operations are independent of mode selection. The Boundary-Scan mode in Virtex-5 devices overrides other mode selections. For this reason, Boundary-Scan instructions using the Boundary-Scan register (SAMPLE/PRELOAD, INTEST, and EXTEST) must not be performed during configuration. All instructions except the user-defined instructions are available before a Virtex-5 device is configured. After configuration, all instructions are available.

JSTART and JSHUTDOWN are instructions specific to the Virtex-5 architecture and configuration flow. In Virtex-5 devices, the TAP controller is not reset by the PROGRAM_B pin and can only be reset by bringing the controller to the TLR state. The TAP controller is reset on power up.

For details on the standard Boundary-Scan instructions EXTEST, INTEST, and BYPASS, refer to the IEEE Standard.

Boundary-Scan Architecture

Virtex-5 device registers include all registers required by the IEEE 1149.1 Standard. In addition to the standard registers, the family contains optional registers for simplified testing and verification (Table 3-2).

Table 3-2: **Virtex-5 Device JTAG Registers**

Register Name	Register Length	Description
Boundary-Scan Register	3 bits per I/O	Controls and observes input, output, and output enable
Instruction Register	10 or 14 bits	Holds current instruction OPCODE and captures internal device status
BYPASS Register	1 bit	Bypasses the device
Identification Register	32 bits	Captures the Device ID
JTAG Configuration Register	32 bits	Allows access to the configuration bus when using the CFG_IN or CFG_OUT instructions
USERCODE Register	32 bits	Captures the user-programmable code
User-Defined Registers (USER1, USER2, USER3, and USER4)	Design-specific	Design-specific

Boundary-Scan Register

The test primary data register is the Boundary-Scan register. Boundary-Scan operation is independent of individual IOB configurations. Each IOB, bonded or unbonded, starts as bidirectional with 3-state control. Later, it can be configured to be an input, output, or 3-state only. Therefore, three data register bits are provided per IOB (Figure 3-3).

When conducting a data register (DR) operation, the DR captures data in a parallel fashion during the CAPTURE-DR state. The data is then shifted out and replaced by new data during the SHIFT-DR state. For each bit of the DR, an update latch is used to hold the input data stable during the next SHIFT-DR state. The data is then latched during the UPDATE-DR state when TCK is Low.

The update latch is opened each time the TAP controller enters the UPDATE-DR state. Care is necessary when exercising an INTEST or EXTEST to ensure that the proper data has been latched before exercising the command. This is typically accomplished by using the SAMPLE/PRELOAD instruction.

Internal pull-up and pull-down resistors should be considered when test vectors are being developed for testing opens and shorts. The HSWAPEN pin determines whether the IOB has a pull-up resistor. Figure 3-3 is a representation of Virtex-5 Boundary-Scan architecture.