Spartan-6 FPGA Unique Device Identifier (Device DNA)

Spartan-6 FPGAs contain an embedded, unique device identifier (device DNA). The identifier is nonvolatile, permanently programmed into the FPGA, and is unchangeable, making it tamper resistant.

The FPGA application accesses the identifier value using the Device DNA Access Port (DNA_PORT) design primitive, shown in Figure 5-13.

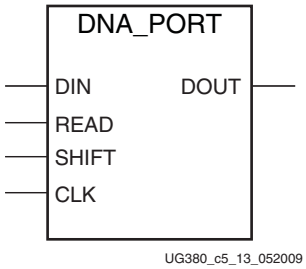

Figure 5-13: **Spartan-6 FPGA DNA_PORT Design Primitive**

Identifier Value

As shown in Figure 5-14, the device DNA value is 57 bits long. The two most-significant bits are always 1 and 0. The remaining 55 bits are unique to a specific Spartan-6 FPGA.

Operation

Figure 5-14 shows the general functionality of the DNA_PORT design primitive. An FPGA application must first instantiate the DNA_PORT primitive, shown in Figure 5-13, within a design.

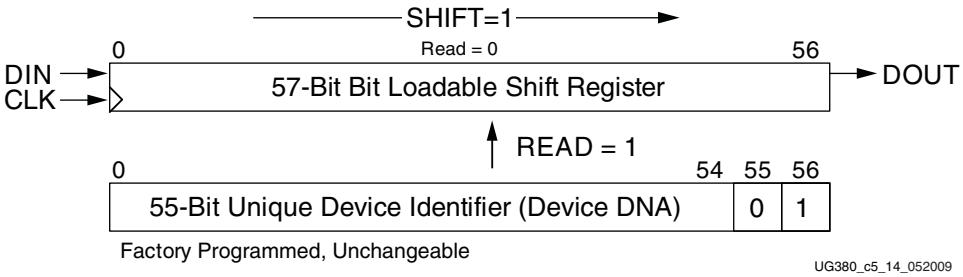

Figure 5-14: **DNA_PORT Operation**

To read the device DNA, the FPGA application must first transfer the identifier value into the DNA_PORT output shift register. The READ input must be asserted during a rising edge of CLK, as shown in Table 5-51. This action parallel loads the output shift register with all 57 bits of the identifier. Because bit 56 of the identifier is always 1, the DOUT output is also 1. The READ operation overrides a SHIFT operation.

To continue reading the identifier values, SHIFT must be asserted, followed by a rising edge of CLK, as shown in Table 5-51. This action causes the output shift register to shift its contents toward the DOUT output. The value on the DIN input is shifted into the shift register.

A Low-to-High transition on SHIFT should be avoided when CLK is High because this causes a spurious initial clock edge. Ideally, SHIFT should only be asserted when CLK is Low or on a falling edge of CLK.

If both READ and SHIFT are Low, the output shift register holds its value and DOUT remains unchanged.

Table 5-51: **DNA_PORT Operations**

Operation	DIN	READ	SHIFT	CLK	Shift Register	DOUT
HOLD	X	0	0	X	Hold previous value	Hold previous value
READ	X	1	X	↑	Parallel load with 57-bit ID	Bit 56 of identifier, which is always 1
SHIFT	DIN	0	1	↑	Shift DIN into bit 0, shift contents of Shift Register toward DOUT	Bit 56 of Shift Register

Notes:

X = Don't care
↑ = Rising clock edge

Identifier Memory Specifications

The unique FPGA identifier value is retained for a minimum of ten years of continuous usage under worst-case recommended operating conditions. The identifier can be read, using the READ operation defined in Table 5-51, a minimum of 30 million cycles, which roughly correlates to one read operation every 11 seconds for the operating lifetime of the Spartan-6 FPGA.

Extending Identifier Length

As shown in Figure 5-15, most applications that use the DNA_PORT primitive tie the DIN data input to a static value.

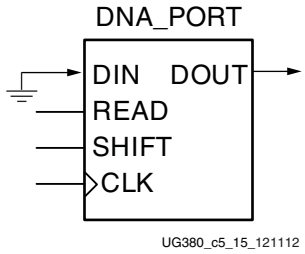

Figure 5-15: **Shift in Constant**

As shown in Figure 5-16, the length of the identifier can be extended by feeding the DOUT serial output port back into the DIN serial input port. This way, the identifier can be extended to any possible length. However, there are still only 55 unique bits, with a 57-bit repeating pattern. A buffer is included in Figure 5-16 to demonstrate a user inserting logic for the user's DNA logic extension or delay for the loopback to meet hold time requirements.

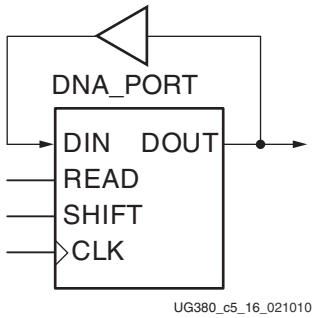

Figure 5-16: **Circular Shift**

It is also possible to add additional bits to the identifier using FPGA logic resources. As shown in Figure 5-17, the FPGA application can insert additional bits via the DNA_PORT DIN serial input. The additional bits provided by the logic resources could take the form of an additional fixed value or a variable computed from the device DNA.

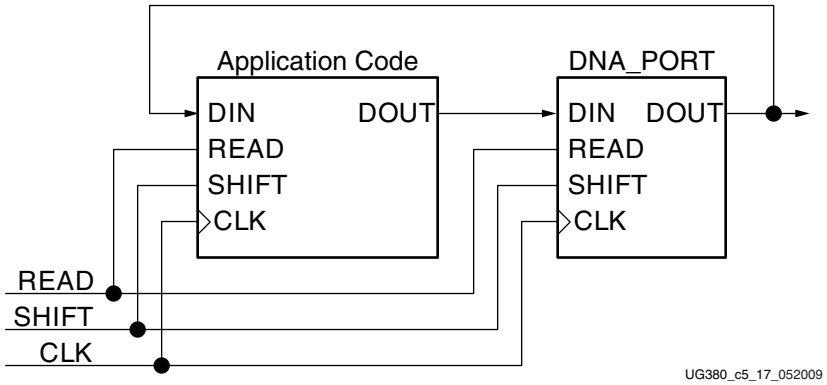

Figure 5-17: **Bitstream Specific Code**

JTAG Access to Device Identifier

The FPGA's internal device identifier, plus any values shifted in on the DIN input, can be read via the JTAG port using the private ISC_DNA command. This requires the ISC_ENABLE to be loaded before the ISC_DNA command is issued.

Bit 56 of the identifier, shown in Figure 5-14, appears on the TDO JTAG output following the ISC_DNA command when the device enters the Shift-DR state. The remaining Device DNA bits and any data on the input to the register are shifted out sequentially while the JTAG controller is left in the Shift-DR state. When this operation is complete, the ISC_DISABLE command should be issued.

XC3130-3PC68C	2001+	PLCC	2315
XC3130-3PC100C	2001+	PLCC	2315
XC3130-2PQ100I	2001+	LQFP100	2315
XC3130-2PQ100C	2001+	QFP	2315
XC3130-1PQ100I	2001+	QFP	2315
XC3130-1PQ100C	2001+	LQFP100	2315
XC3130-10PQ100C	2001+	QFP	2315
XC3130	2001+	PLCC	2315
XC3128XL-VQ100	2001+	QFP	2315
XC3128XLVQ100	2001+	QFP	2315
XC3128XL-7VQ100C	2001+	QFP	2315
XC3128XL-10VQG100C	2001+	BGA	2315
XC3128XL-10VQ100	2001+	QFP	2315
XC3128XL-10TQG144C	2001+	QFP	2315
XC3128XL-10TQ144I	2001+	QFP	2315
XC3128PQ100	2001+	QFP	2315
XC3124A-3VQ100C	2001+	99	2315
XC3124A-3PQ100I	2001+	原厂原封	2315
XC3120TM-5	2001+	PLCC	2315
XC3120TM-4	2001+	PLCC	2315
XC3120TM-3	2001+	PLCC	2315
XC3120QPQ100	2001+	QFP	2315
XC3120PQ100	2001+	QFP	2315
XC3120PC68-5C	2001+	PLCC68	2315
XC3120ATMPC68AKJ	2001+	PLCC68	2315
XC3120ATM	2001+	PLCC	2315
XC3120A-PQ100AKJ	2001+	QFP-100	2315
XC3120APQ100	2001+	QFP	2315
XC3120APC68-4C	2001+	PLCC68	2315
XC3120APC68	2001+	PLCC	2315
XC3120A-5PQ100I	2001+	LQFP100	2315
XC3120A-5PQ100C	2001+	LQFP100	2315
XC3120A-5PC84I	2001+	PLCC	2315
XC3120A-5PC84C	2001+	PLCC	2315
XC3120A-5PC68C	2001+	PLCC	2315
XC3120A-4PQ100I	2001+	LQFP100	2315
XC3120A-4PQ100C	2001+	QFP100	2315
XC3120A-4PQ100C	2001+	QFP100	2315
XC3120A-4PC84I	2001+	PLCC	2315
XC3120A-4PC84C	2001+	NA	2315
XC3120A-4PC68I	2001+	PLCC68	2315

XC3120A-2PC68C	2001+	PLCC	2315
XC3120A-1PQ100I	2001+	LQFP100	2315
XC3120A-1PQ100C	2001+	LQFP100	2315
XC3120A-1PC84I	2001+	PLCC	2315
XC3120A-1PC84C	2001+	PLCC	2315
XC3120A-1PC68C	2001+	PLCC	2315
XC3120A-09PQ100I	2001+	LQFP100	2315
XC3120A-09PQ100C	2001+	NA	2315
XC3120A-09PG84C	2001+	QFP	2315
XC3120A-09PC84C	2001+	BGA	2315
XC3120A-09PC68C	2001+	NA	2315
XC3120A PC68	2001+	PLCC	2315
XC3120A	2001+	BGA	2315
XC3120-5PQG100I	2001+	QFP	2315
XC3120-5PQG100C	2001+	QFP	2315
XC3120-5PQ100I	2001+	LQFP100	2315
XC3120-5PQ100C	2001+	QFP	2315
XC3120-5PQ100	2001+	原厂原封	2315
XC3120-5PC84I	2001+	PLCC	2315
XC3120-5PC84C	2001+	PLCC	2315
XC3120-5PC68I	2001+	PLCC	2315
XC3120-5PC68C	2001+	BGA	2315
XC3120-5	2001+	PLCC84	2315
XC3120-4PQG100C	2001+	QFP	2315
XC3120-4PQ100I	2001+	LQFP100	2315
XC3120-4PQ100C	2001+	BGA	2315
XC3120-4PQ100	2001+	原厂原封	2315
XC3120-4PC84I	2001+	PLCC	2315
XC3120-4PC68C	2001+	BGA	2315
XC3120-3PQG100I	2001+	QFP	2315
XC3120-3PQG100C	2001+	QFP	2315
XC3120-3PQ100I	2001+	QFP	2315
XC3120-3PQ100C	2001+	QFP	2315
XC3120-3PC84C	2001+	PLCC	2315
XC3120-3PC68I	2001+	PLCC	2315
XC3120-3PC68C	2001+	BGA	2315
XC3120-3PC68	2001+	PLCC	2315
XC31010APQ160	2001+	QFP	2315
XC3100L	2001+	BGA	2315
XC3100A/L	2001+	BGA	2315
XC3100A	2001+	BGA	2315