The user must change the SelectMAP interface from write to read control between steps 10 and 11, and back to write control after step 11, as illustrated in Figure 6-2. The SelectMAP 16-bit data ordering applies to the ICAP interface as shown in Table 2-4, page 39 and Table 2-5, page 40.
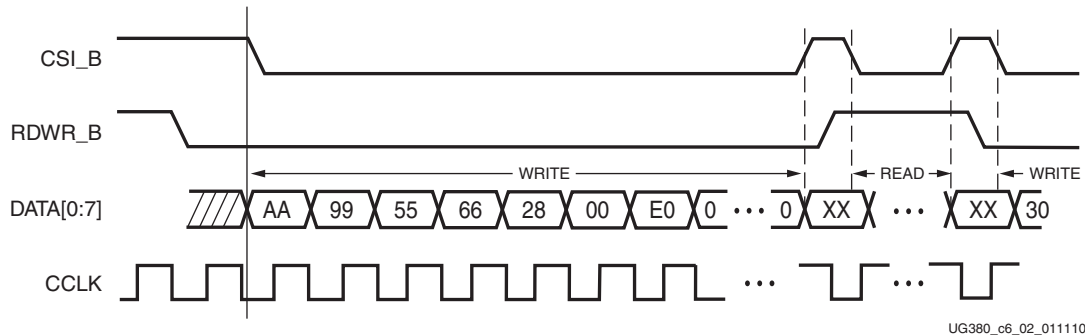

Figure 6-2: **8-Bit SelectMAP Status Register Read**

To read registers other than STAT, the address specified in the Type-1 packet header in step 2 of Table 6-1 should be modified and the word count changed if necessary. Reading from the FDRO register is a special case that is described in Configuration Memory Read Procedure (SelectMAP).

Configuration Memory Read Procedure (SelectMAP)

The process for reading configuration memory from the FDRO register is similar to the process for reading from other registers. Additional steps are needed to accommodate the configuration logic. Configuration data coming from the FDRO register passes through the frame buffer. The first frame of readback data should be discarded. After changing the FAR or beginning to read a different frame type, it is necessary to send the DESYNC command and a new synchronization word prior to starting another read operation.

1. Write the dummy and synchronization words to the device.

2. Write one NOOP command.

3. Write the Shutdown command, and write NOOP commands.

4. Write the RCRC command, and write one NOOP command.

5. Write the AGHIGH command to disable the interconnect, and write one NOOP command.

6. Set the frame length register.

7. Write the Starting Frame Address to the FAR (typically `0x00000000`).

8. Write the RCFG command to the CMD register.

9. Write the *read FDRO register* packet header to the device. The FDRO read length is given by:

   FDRO Read Length = (words per frame) x (frames to read + 1) + 1

   One extra frame is read to account for the frame buffer. Users should strobe readback data while DOUT_BUSY is Low. The frame buffer produces one dummy frame at the beginning of the read. Also, one extra word is read in SelectMap8 mode.

10. Write to the device to flush the packet buffer.

芯片详细信息

Manufacturer Part Number: XC2VP2-6FGG256C	Pbfree Code: ✅ Yes	Rohs Code: ✅ Yes	Part Life Cycle Code: Obsolete
Ihs Manufacturer: XILINX INC	Part Package Code: BGA	Package Description: BGA, BGA256,16X16,40	Pin Count: 256
Reach Compliance Code: compliant	ECCN Code: EAR99	HTS Code: 8542.39.00.01	Factory Lead Time: 12 Weeks
Manufacturer: Xilinx	Risk Rank: 8.55	Clock Frequency-Max: 1200 MHz	Combinatorial Delay of a CLB-Max: 0.32 ns
JESD-30 Code: S-PBGA-B256	JESD-609 Code: e1	Length: 17 mm	Moisture Sensitivity Level: 3
Number of CLBs: 352	Number of Inputs: 140	Number of Logic Cells: 3168	Number of Outputs: 140
Number of Terminals: 256	Operating Temperature-Max: 85 °C	Organization: 352 CLBS	Package Body Material: PLASTIC/EPOXY
Package Code: BGA	Package Equivalence Code: BGA256,16X16,40	Package Shape: SQUARE	Package Style: GRID ARRAY
Peak Reflow Temperature (Cel): 260	Power Supplies: 1.5,1.5/3.3,2/2.5,2.5 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified
Seated Height-Max: 2 mm	Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.575 V	Supply Voltage-Min: 1.425 V
Supply Voltage-Nom: 1.5 V	Surface Mount: YES	Technology: CMOS	Temperature Grade: OTHER
Terminal Finish: Tin/Silver/Copper (Sn95.5Ag4.0Cu0.5)	Terminal Form: BALL	Terminal Pitch: 1 mm	Terminal Position: BOTTOM
Time@Peak Reflow Temperature-Max (s): 30	Width: 17 mm		

Reconfiguration and MultiBoot

MultiBoot Overview

Because Spartan®-6 FPGAs are reprogrammable in the system, some applications reload the FPGA with one or more bitstream images during normal operation. In this way, a single smaller FPGA, reprogrammed multiple times, replaces a much larger and more expensive ASIC or FPGA programmed just once.

A variety of methods can be used to reprogram the FPGA during normal operation. The downloaded configuration modes inherently provide this capability. Via an external "intelligent agent," such as a processor, microcontroller, computer, or tester, an FPGA can be reprogrammed numerous times. The downloaded modes are available on all Spartan-6 FPGA families.

Spartan-6 FPGAs include a capability called MultiBoot that allows the FPGA to selectively reprogram and reload its bitstream from an attached external memory. The MultiBoot feature allows the FPGA application to load two or more FPGA bitstreams under the control of the FPGA application. The FPGA application triggers a MultiBoot operation, causing the FPGA to reconfigure from a different configuration bitstream. After a MultiBoot operation is triggered, the FPGA restarts its configuration process as usual. The INIT_B pin pulses Low while the FPGA clears its configuration memory, and the DONE output remains Low until the MultiBoot operation successfully completes.

MultiBoot is supported in SPI x1, x2, x4, and BPI configuration modes.

Fallback MultiBoot

Fallback Behavior

Spartan-6 FPGAs have dedicated MultiBoot logic, which is used for both fallback and MultiBoot (IPROG) reconfiguration. When fallback or IPROG happens, an internally generated pulse resets the entire configuration logic, except for the dedicated MultiBoot logic and the BOOTSTS, MODE, and GENERAL1.5 registers. See Figure 7-1. This reset pulse pulls INIT_B and DONE Low, and restarts the configuration process by clearing configuration memory.
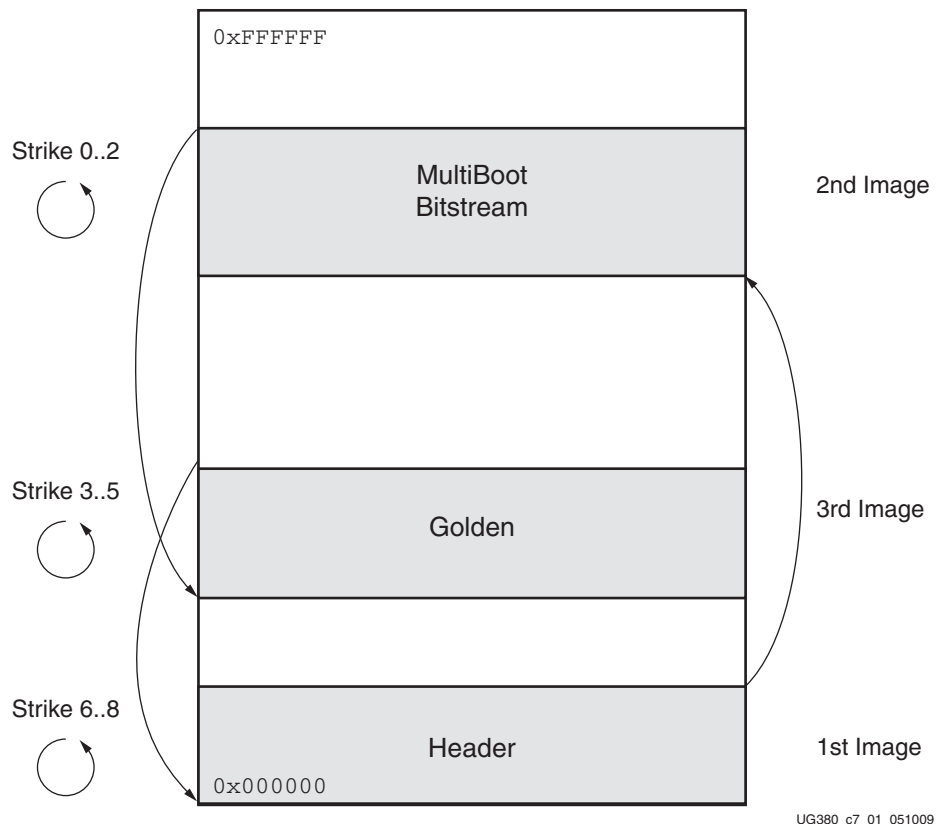

Figure 7-1: **MultiBoot Logic**

During configuration, a CRC error or a watchdog timer time-out error can trigger fallback. The watchdog timer is only active in master configuration modes. The time-out value is user configurable using the BitGen **–g TIMER_CFG** switch. The switch is followed by a 16-bit value (greater than 16h'0201) indicating the number of configuration clocks allowed before detection of the Sync word times out.

During fallback reconfiguration, the FPGA increments the strike count, stored in the BOOTSTS register, and continues reconfiguration if the strike count is less than the limit permitted for that image. If the limit is not reached, the FPGA checks the NEW_MODE bit in the MODE register. If this value is 0, the device uses the configuration mode defined by the mode pins. If the value is 1, the device uses the configuration mode defined in the BOOTMODE bits in the MODE register. The NEW_MODE register is set by the BitGen option **–g Next_Config_New_Mode:Yes**. The BOOTMODE bits are set by the BitGen option **–g Next_Config_Boot_Mode**.

XC3S1000-5CPG132C	2001+	BGA	2315
XC3S1000-5CP132I	2001+	BGA	2315
XC3S1000-5CP132C	2001+	BGA	2315
XC3S1000-4VQG100I	2001+	BGA	2315
XC3S1000-4VQG100C	2001+	BGA	2315
XC3S1000-4VQ100I	2001+	BGA	2315
XC3S1000-4VQ100C	2001+	BGA	2315
XC3S1000-4TQG144I	2001+	BGA	2315
XC3S1000-4TQG144C	2001+	BGA	2315
XC3S1000-4TQ144I	2001+	BGA	2315
XC3S1000-4TQ144C	2001+	BGA	2315
XC3S1000-4PQG208I	2001+	BGA	2315
XC3S1000-4PQG208C	2001+	BGA	2315
XC3S1000-4PQ208I	2001+	BGA	2315
XC3S1000-4PQ208C	2001+	BGA	2315
XC3S1000-4IFG256EGQ	2001+	BGA	2315
XC3S1000-4FTG256I	2001+	BGA	2315
XC3S10004FTG256I	2001+	NA	2315
XC3S1000-4FTG256C	2001+	BGA256	2315
XC3S1000-4FTG256C	2001+	BGA256	2315
XC3S10004FTG256C	2001+	BGA	2315
XC3S1000-4FTG256	2001+	BGA	2315
XC3S1000-4FT256I	2001+	BGA	2315
XC3S10004FT256I	2001+	BGA	2315
XC3S1000-4FT256C0961	2001+	BGA	2315
XC3S1000-4FT256C	2001+	BGA	2315
XC3S10004FT256C	2001+	BGA	2315
XC3S1000-4FI256I	2001+	BGA	2315
XC3S1000-4FGG768C	2001+	BGA	2315
XC3S1000-4FGG676I	2001+	BGA	2315
XC3S1000-4FGG676C	2001+	BGA	2315
XC3S1000-4FGG456I	2001+	BGA	2315
XC3S1000-4FGG456I	2001+	FPGA456	2315
XC3S1000-4FGG456C	2001+	BGA320	2315
XC3S1000-4FGG456C	2001+	BGA320	2315
XC3S10004FGG456C	2001+	NA	2315
XC3S1000-4FGG320I	2001+	BGA320	2315
XC3S1000-4FGG320I	2001+	BGA320	2315
XC3S1000-4FGG320C	2001+	BGA676	2315
XC3S1000-4FGG320C	2001+	BGA676	2315
XC3S1000-4FGG256C	2001+	BGA	2315