Spartan-3 FPGA Family: Pinout Descriptions

Introduction

This data sheet module describes the various pins on a Spartan®-3 FPGA and how they connect to the supported component packages.

- The Pin Types section categorizes all of the FPGA pins by their function type.
- The Pin Definitions section provides a top-level description for each pin on the device.
- The Detailed, Functional Pin Descriptions section offers significantly more detail about each pin, especially for the dual- or special-function pins used during device configuration.
- Some pins have associated behavior that is controlled by settings in the configuration bitstream. These options are described in the Bitstream Options section.
- The Package Overview section describes the various packaging options available for Spartan-3 FPGAs. Detailed pin list tables and footprint diagrams are provided for each package solution.

Pin Descriptions

Pin Types

A majority of the pins on a Spartan-3 FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3 device packages, as outlined in Table 69. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 69: **Types of Pins on Spartan-3 FPGAs**

Pin Type/ Color Code	Description	Pin Name
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO, IO_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. There are 12 dual-purpose configuration pins on every package. The INIT_B pin has an internal pull-up resistor to VCCO_4 or VCCO_BOTTOM during configuration.	IO_Lxxy_#/DIN/D0, IO_Lxxy_#/D1, IO_Lxxy_#/D2, IO_Lxxy_#/D3, IO_Lxxy_#/D4, IO_Lxxy_#/D5, IO_Lxxy_#/D6, IO_Lxxy_#/D7, IO_Lxxy_#/CS_B, IO_Lxxy_#/RDWR_B, IO_Lxxy_#/BUSY/DOUT, IO_Lxxy_#/INIT_B
CONFIG	Dedicated configuration pin. Not available as a user-I/O pin. Every package has seven dedicated configuration pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	CCLK, DONE, M2, M1, M0, PROG_B, HSWAP_EN
JTAG	Dedicated JTAG pin. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX and have a dedicated internal pull-up resistor to VCCAUX during configuration.	TDI, TMS, TCK, TDO
DCI	Dual-purpose pin that is either a user-I/O pin or used to calibrate output buffer impedance for a specific bank using Digital Controlled Impedance (DCI). There are two DCI pins per I/O bank.	IO/VRN_# IO_Lxxy_#/VRN_# IO/VRP_# IO_Lxxy_#/VRP_#

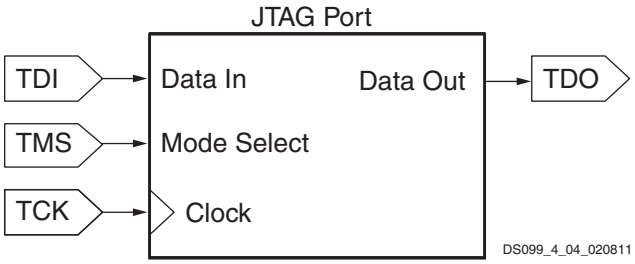

Figure 43: **JTAG Port**

IDCODE Register

Spartan-3 FPGAs contain a 32-bit identification register called the IDCODE register, as defined in the IEEE 1149.1 JTAG standard. The fixed value electrically identifies the manufacture (Xilinx) and the type of device being addressed over a JTAG chain. This register allows the JTAG host to identify the device being tested or programmed via JTAG. See Table 78.

Using JTAG Port After Configuration

The JTAG port is always active and available before, during, and after FPGA configuration. Add the BSCAN_SPARTAN3 primitive to the design to create user-defined JTAG instructions and JTAG chains to communicate with internal logic.

Furthermore, the contents of the User ID register within the JTAG port can be specified as a Bitstream Generation option. By default, the 32-bit User ID register contains `0xFFFFFFFF`.

Table 78: **Spartan-3 JTAG IDCODE Register Values (hexadecimal)**

Part Number	IDCODE Register
XC3S50	0x0140C093
XC3S200	0x01414093
XC3S400	0x0141C093
XC3S1000	0x01428093
XC3S1500	0x01434093
XC3S2000	0x01440093
XC3S4000	0x01448093
XC3S5000	0x01450093

Precautions When Using the JTAG Port in 3.3V Environments

The JTAG port is powered by the +2.5V VCCAUX power supply. When connecting to a 3.3V interface, the JTAG input pins must be current-limited using a series resistor. Similarly, the TDO pin is a CMOS output powered from +2.5V. The TDO output can directly drive a 3.3V input but with reduced noise immunity. See 3.3V-Tolerant Configuration Interface, page 47. See also XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional details.

The following interface precautions are recommended when connecting the JTAG port to a 3.3V interface.

- Avoid actively driving the JTAG input signals High with 3.3V signal levels. If required in the application, use series current-limiting resistors to keep the current below 10 mA per pin.
- If possible, drive the FPGA JTAG inputs with drivers that can be placed in high-impedance (Hi-Z) after using the JTAG port. Alternatively, drive the FPGA JTAG inputs with open-drain outputs, which only drive Low. In both cases, pull-up resistors are required. The FPGA JTAG pins have pull-up resistors to VCCAUX before configuration and optional pull-up resistors after configuration, controlled by Bitstream Options, page 125.

VREF: User I/O or Input Buffer Reference Voltage for Special Interface Standards

These pins are individual user-I/O pins unless collectively they supply an input reference voltage, VREF_#, for any SSTL, HSTL, GTL, or GTLP I/Os implemented in the associated I/O bank. The '#' character in the pin name represents an integer, 0 through 7, that indicates the associated I/O bank.

The VREF function becomes active for this pin whenever a signal standard requiring a reference voltage is used in the associated bank. If used as a user I/O, then each pin behaves as an independent I/O described in the I/O type section. If used for a reference voltage within a bank, then *all* VREF pins within the bank must be connected to the same reference voltage.

Spartan-3 devices are designed and characterized to support certain I/O standards when VREF is connected to +1.25V, +1.10V, +1.00V, +0.90V, +0.80V, and +0.75V. During configuration, the VREF pins behave exactly like user-I/O pins.

If designing for footprint compatibility across the range of devices in a specific package, and if the VREF_# pins within a bank connect to an input reference voltage, then also connect any N.C. (not connected) pins on the smaller devices in that package to the input reference voltage. More details are provided later for each package type.

N.C. Type: Unconnected Package Pins

Pins marked as "N.C." are unconnected for the specific device/package combination. For other devices in this same package, this pin may be used as an I/O or VREF connection. In both the pinout tables and the footprint diagrams, unconnected pins are noted with either a black diamond symbol (◆) or a black square symbol (■).

If designing for footprint compatibility across multiple device densities, check the pin types of the other Spartan-3 devices available in the same footprint. If the N.C. pin matches to VREF pins in other devices, and the VREF pins are used in the associated I/O bank, then connect the N.C. to the VREF voltage source.

VCCO Type: Output Voltage Supply for I/O Bank

Each I/O bank has its own set of voltage supply pins that determines the output voltage for the output buffers in the I/O bank. Furthermore, for some I/O standards such as LVCMOS, LVCMOS25, LVTTL, etc., VCCO sets the input threshold voltage on the associated input buffers.

Spartan-3 devices are designed and characterized to support various I/O standards for VCCO values of +1.2V, +1.5V, +1.8V, +2.5V, and +3.3V.

Most VCCO pins are labeled as VCCO_# where the '#' symbol represents the associated I/O bank number, an integer ranging from 0 to 7. In the 144-pin TQFP package (TQ144) however, the VCCO pins along an edge of the device are combined into a single VCCO input. For example, the VCCO inputs for Bank 0 and Bank 1 along the top edge of the package are combined and relabeled VCCO_TOP. The bottom, left, and right edges are similarly combined.

In Serial configuration mode, VCCO_4 must be at a level compatible with the attached configuration memory or data source. In Parallel configuration mode, both VCCO_4 and VCCO_5 must be at the same compatible voltage level.

All VCCO inputs to a bank must be connected together and to the voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in XAPP623: *Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors*.

VCCINT Type: Voltage Supply for Internal Core Logic

Internal core logic circuits such as the configurable logic blocks (CLBs) and programmable interconnect operate from the VCCINT voltage supply inputs. VCCINT must be +1.2V.

All VCCINT inputs must be connected together and to the +1.2V voltage supply. Furthermore, there must be sufficient supply decoupling to guarantee problem-free operation, as described in XAPP623.

VCCAUX Type: Voltage Supply for Auxiliary Logic

The VCCAUX pins supply power to various auxiliary circuits, such as to the Digital Clock Managers (DCMs), the JTAG pins, and to the dedicated configuration pins (CONFIG type). VCCAUX must be +2.5V.

芯片详细信息

Manufacturer Part Number: XC2VP2-6FG256I	Pbfree Code: No	Rohs Code: No	Part Life Cycle Code: Obsolete
Ihs Manufacturer: XILINX INC	Part Package Code: BGA	Package Description: BGA, BGA256,16X16,40	Pin Count: 256
Reach Compliance Code: not_compliant	ECCN Code: EAR99	HTS Code: 8542.39.00.01	Factory Lead Time: 12 Weeks
Manufacturer: Xilinx	Risk Rank: 5.77	Clock Frequency-Max: 1200 MHz	Combinatorial Delay of a CLB-Max: 0.32 ns
JESD-30 Code: S-PBGA-B256	JESD-609 Code: e0	Length: 17 mm	Moisture Sensitivity Level: 3
Number of CLBs: 352	Number of Inputs: 140	Number of Logic Cells: 3168	Number of Outputs: 140
Number of Terminals: 256	Organization: 352 CLBS	Package Body Material: PLASTIC/EPOXY	Package Code: BGA
Package Equivalence Code: BGA256,16X16,40	Package Shape: SQUARE	Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 225
Power Supplies: 1.5,1.5/3.3,2/2.5,2.5 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 2 mm
Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.575 V	Supply Voltage-Min: 1.425 V	Supply Voltage-Nom: 1.5 V
Surface Mount: YES	Technology: CMOS	Terminal Finish: Tin/Lead (Sn63Pb37)	Terminal Form: BALL
Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 30	Width: 17 mm

XC3490A-5PQ208C	2001+	BGA	2315
XC3490A-5213PQ160C	2001+	QFP	2315
XC3490A-5204PQ208C	2001+	QFP2828-208	2315
XC3490A-5180PQ160C	2001+	QFP	2315
XC3490A-5179PQ160C	2001+	QFP	2315
XC3490A-5156PQ160C	2001+	QFP	2315
XC3490A-5155PQ160C	2001+	QFP	2315
XC3490A-5154PQ160C	2001+	QFP	2315
XC3490	2001+	QFP	2315
XC3430ATM-PC44C-5203	2001+	PLCC44	2315
XC3430A-PC44C	2001+	PLCC-44	2315
XC3430APC44	2001+	PLCC	2315
XC3430A	2001+	PLCC-44	2315
XC342-70PG132C	2001+	PGA	2315
XC3412APC84-3C	2001+	PLCC84	2315
XC34114P	2001+	BGA	2315
XC3405-PQ160C	2001+	QFP	2315
XC3390TMPQ160	2001+	QFP	2315
XC3390TM-PC84C-5240	2001+	PLCC84	2315
XC3390TMPC84	2001+	PLCC	2315
XC3390TM-5229PC84C	2001+	PLCC	2315
XC3390TM-5229PC84	2001+	PLCC	2315
XC3390TM	2001+	QFP	2315
XC3390PQG160C	2001+	QFP	2315
XC3390PQ160I5159	2001+	QFP	2315
XC3390PQ160I-5029	2001+	QFP	2315
XC3390PQ160I	2001+	QFP	2315
XC3390PQ160C-5029	2001+	QFP160	2315
XC3390PQ160C5029	2001+	BGA	2315
XC3390-PQ160C	2001+	QFP	2315
XC3390PQ160C	2001+	QFP	2315
XC3390PQ160-5029	2001+	BGA	2315
XC3390PQ160	2001+	QFP	2315
XC3390-PC84I	2001+	PLCC	2315
XC3390PC84C-5240	2001+	BGA	2315
XC3390-PC84C	2001+	PLCC	2315
XC3390PC84	2001+	PLCC84	2315
XC3390ATQG176C	2001+	QFP	2315
XC3390ATQ176I	2001+	QFP	2315
XC3390ATQ176C-5518	2001+	TQFP	2315
XC3390ATQ176C	2001+	QFP	2315