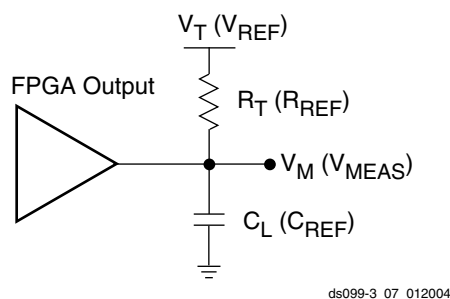## Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 48 presents the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 35. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (e.g., LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.

ds099-3_07_012004

Notes:
1. The names shown in parentheses are used in the IBIS file.

Figure 35: **Output Test Setup**

Table 48: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended						
GTL	0.8	$V_{REF} - 0.2$	$V_{REF} + 0.2$	25	1.2	V_{REF}
GTL_DCI				50	1.2	
GTLP	1.0	$V_{REF} - 0.2$	$V_{REF} + 0.2$	25	1.5	V_{REF}
GTLP_DCI				50	1.5	
HSLVDCI_15	0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	1M	0	0.75
HSLVDCI_18						0.90
HSLVDCI_25						1.25
HSLVDCI_33						1.65
HSTL_I	0.75	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.75	V_{REF}
HSTL_I_DCI						
HSTL_III	0.90	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.5	V_{REF}
HSTL_III_DCI						
HSTL_I_18	0.90	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
HSTL_I_DCI_18						
HSTL_II_18	0.90	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
HSTL_II_DCI_18						

Table 48: **Test Methods for Timing Measurement at I/Os** *(Cont'd)*

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
DIFF_SSTL2_II	-	$V_{ICM} - 0.75$	$V_{ICM} + 0.75$	50	1.25	V_{ICM}
DIFF_SSTL2_II_DCI						

Notes:

1. Descriptions of the relevant symbols are as follows:
   VREF – The reference voltage for setting the input switching threshold
   VICM – The common mode input voltage
   VM – Voltage of measurement point on signal transition
   VL – Low-level test voltage at Input pin
   VH – High-level test voltage at Input pin
   RT – Effective termination resistance, which takes on a value of 1MW when no parallel termination is required
   VT – Termination voltage
2. The load capacitance (CL) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS Models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 48, V_T, R_T, and V_M. Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link.

Simulate delays for a given application according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 35. Use parameter values V_T, R_T, and V_M from Table 48. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase (or decrease) in delay should be added to (or subtracted from) the appropriate Output standard adjustment (Table 47) to yield the worst-case delay of the PCB trace.

Simultaneously Switching Output Guidelines

This section provides guidelines for the maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins, of a given output signal standard, that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 49 and Table 50 provide the essential SSO guidelines. For each device/package combination, Table 49 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and will possibly not match the physical number of pairs. For each output signal standard and drive strength, Table 50 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The Table 50 guidelines are categorized by package style. Multiply the appropriate numbers from Table 49 and Table 50 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines may result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

$$\text{SSO}_{MAX}/\text{IO Bank} = \text{Table 49} \times \text{Table 50}$$

The recommended maximum SSO values assume that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The number of SSOs allowed for quad-flat packages (VQ, TQ, PQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 49: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	VQ100	CP132[1][2]	TQ144[1]	PQ208	FT256	FG320	FG456	FG676	FG900	FG1156[2]
XC3S50	1	1.5	1.5	2	–	–	–	–	–	–
XC3S200	1	–	1.5	2	3	–	–	–	–	–
XC3S400	–	–	1.5	2	3	3	5	–	–	–
XC3S1000	–	–	–	–	3	3	5	5	–	–
XC3S1500	–	–	–	–	–	3	5	6	–	–
XC3S2000	–	–	–	–	–	–	5	6	9	–
XC3S4000	–	–	–	–	–	–	–	6	10	12
XC3S5000	–	–	–	–	–	–	–	6	10	12

Notes:

产品种类:	FPGA - 现场可编程门阵列	✅
产品:	Virtex-II Pro	☐
系列:	XC2VP2	☐
逻辑元件数量:	3168 LE	☐
自适应逻辑模块 - ALM:	1408 ALM	☐
嵌入式内存:	216 kbit	☐
输入/输出端数量:	140 I/O	☐
工作电源电压:	1.5 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 85 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-256	☐
数据速率:	6.25 Gb/s	
商标:	Xilinx	
分布式RAM:	44 kbit	
内嵌式块RAM - EBR:	216 kbit	
最大工作频率:	350 MHz	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	352 LAB	
收发器数量:	4 Transceiver	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	90	
子类别:	Programmable Logic ICs	
商标名:	Virtex	

XC3390ATQ144C-5512	2001+	TQFP	2315
XC3390ATQ144	2001+	TQFP	2315
XC3390ATM	2001+	PLCC84	2315
XC3390APQG160C	2001+	QFP	2315
XC3390APQ160I	2001+	QFP	2315
XC3390APQ160C-5231	2001+	QFP	2315
XC3390APQ160C	2001+	QFP	2315
XC3390APQ160	2001+	QFP	2315
XC3390-5PQ160I	2001+	QFP	2315
XC3390-5PQ160C	2001+	QFP	2315
XC3390-5PC84C	2001+	PLCC	2315
XC3390-50PQ160C	2001+	QFP2828-160	2315
XC3390-5073PP175C	2001+	PBGA	2315
XC3390-5001PP175C	2001+	PGA	2315
XC3390-5000PP175C	2001+	PGA	2315
XC3390-10PQ160C	2001+	QFP	2315
XC3390	2001+	BGA	2315
XC3342TMPC84C-5032	2001+	PLCC	2315
XC3342TM-PC84C	2001+	PLCC	2315
XC3342TMPC84C	2001+	PLCC	2315
XC3342TMPC84	2001+	PLCC	2315
XC3342TM-5277PC84	2001+	PLCC	2315
XC3342TM-5120PC84	2001+	PLCC	2315
XC3342TM-5060PC84	2001+	PLCC	2315
XC3342TM-5032PC84-15	2001+	PLCC	2315
XC3342TM-5018PC84	2001+	PLCC	2315
XC3342TM-5012PC84	2001+	PLCC	2315
XC3342TM-35ABB	2001+	PLCC	2315
XC3342PQG100C	2001+	QFP	2315
XC3342PQ100I-5088	2001+	NA	2315
XC3342PQ100I5081	2001+	BGA	2315
XC3342-PQ100I-5077	2001+	QFP100	2315
XC3342-PQ100I	2001+	BGA	2315
XC3342PQ100I	2001+	QFP	2315
XC3342PQ100C5500	2001+	BGA	2315
XC3342-PQ100C-5080	2001+	QFP	2315
XC3342-PQ100C5051	2001+	BGA	2315
XC3342PQ100C-5051	2001+	QFP	2315
XC3342PQ100C-5033	2001+	NA	2315
XC3342PQ100C-5014	2001+	QFP	2315
XC3342PQ100C-5002	2001+	QFP	2315