Chapter 1

VC707 Evaluation Board Features

Overview

The VC707 evaluation board for the Virtex®-7 FPGA provides a hardware environment for developing and evaluating designs targeting the Virtex-7 XC7VX485T-2FFG1761C FPGA. The VC707 board provides features common to many embedded processing systems, including a DDR3 SODIMM memory, an 8-lane PCI Express® interface, a tri-mode Ethernet PHY, general purpose I/O, and two UART interfaces. Other features can be added by using mezzanine cards attached to either of two VITA-57 FPGA mezzanine connectors (FMC) provided on the board. Two high pin count (HPC) FMCs are provided. See VC707 Board Features for a complete list of features. The details for each feature are described in Feature Descriptions.

Additional Information

See Appendix G, Additional Resources for references to documents, files and resources relevant to the VC707 board.

VC707 Board Features

- Virtex-7 XC7VX485T-2FFG1761C FPGA
- 1 GB DDR3 memory SODIMM
- 128 MB Linear byte peripheral interface (BPI) Flash memory
- USB 2.0 ULPI Transceiver
- Secure Digital (SD) connector
- USB JTAG through Digilent module
- Clock Generation
  - Fixed 200 MHz LVDS oscillator (differential)
  - I^2C programmable LVDS oscillator (differential)
  - SMA connectors (differential)
  - SMA connectors for GTX transceiver clocking
- GTX transceivers
  - FMC1 HPC connector (eight GTX transceivers)
  - FMC2 HPC connector (eight GTX transceiver)
  - SMA connectors (one pair each for TX, RX, and REFCLK)
  - PCI Express (eight lanes)
  - Small form-factor pluggable plus (SFP+) connector
  - Ethernet PHY SGMII interface (RJ-45 connector)

- PCI Express endpoint connectivity
  - Gen1 8-lane (x8)
  - Gen2 8-lane (x8)
- SFP+ Connector
- 10/100/1000 tri-speed Ethernet PHY
- USB-to-UART bridge
- HDMI™ codec
- I^2C bus
  - I^2C MUX
  - I^2C EEPROM (1 KB)
  - USER I^2C programmable LVDS oscillator
  - DDR3 SODIMM socket
  - HDMI codec
  - FMC1 HPC connector
  - FMC2 HPC connector
  - SFP+ connector
  - I^2C programmable jitter-attenuating precision clock multiplier
- Status LEDs
  - Ethernet status
  - Power good
  - FPGA INIT
  - FPGA DONE
- User I/O
  - User LEDs (eight GPIO)
  - User pushbuttons (five directional)
  - CPU reset pushbutton
  - User DIP switch (8-pole GPIO)
  - User SMA GPIO connectors (one pair)
  - LCD character display (16 characters x 2 lines)
- Switches
  - Power on/off slide switch
  - FPGA_PROB_B pushbutton
  - Configuration mode DIP switch
- VITA 57.1 FMC1 HPC Connector
- VITA 57.1 FMC2 HPC Connector
- Power management
  - PMBus voltage and current monitoring through TI power controller
- XADC header
- Configuration options
  - Linear BPI Flash memory

Table 1-29: **Onboard Power System Devices *(Cont'd)***

Device Type	Reference Designator	Description	Power Rail Net Name	Power Rail Voltage	Schematic Page
TPS51200DR	U33	Tracking Regulator, 3A	VTTDDR	0.75V	46

Notes:
1. See Table 1-30.
2. See Table 1-31.
3. See Table 1-34.

Data sheets for the Texas Instruments controller and regulators are available at the Texas Instruments website [Ref 25], and for the Analog Devices ADP123 at [Ref 26].

FMC_VADJ Voltage Control

The FMC_VADJ rail is set to 1.8V. When the VC707 board is powered on, the state of the FMC_VADJ_ON_B signal wired to header J51 is sampled by the TI UCD9248 controller U42. If a jumper is installed on J51 signal FMC_VADJ_ON_B is held low, and the TI controller U42 energizes the FMC_VADJ rail at power on.

Because the rail turn on decision is made at power on time based on the presence of the J51 jumper, removing the jumper at J51 after the board is powered up does not affect the 1.8V power delivered to the FMC_VADJ rail and it remains on.

A jumper installed at J51 is the default setting.

If a jumper is not installed on J51, signal FMC_VADJ_ON_B is high, and the VC707 board does not energize the FMC_VADJ 1.8V at power on. In this mode the user can control when to turn on FMC_VADJ and to what voltage level (1.2V, 1.5V, 1.8V). With FMC_VADJ off, the FPGA still configures and has access to the TI controller PMBUS along with the VADJ_ON_B signal. The combination of these allows the user to develop code to command the FMC_VADJ rail to be set to something other than the default setting of 1.8V. After the new FMC_VADJ voltage level has been programmed into TI controller U42, the VADJ_ON_B signal can be driven low by the user logic and the FMC_VADJ rail comes up at the new FMC_VADJ voltage level. Installing a jumper at J51 after a VC707 board powers up in this mode turns on the FMC_VADJ rail.

Documentation describing PMBUS programming for the UCD9248 digital power controller is available at the Texas Instruments website [Ref 25].

Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface. The three onboard TI power controllers (U42 at address 52, U43 at address 53, and U64 at address 54) are wired to the same PMBus. The PMBus connector, J5, is provided for use with the TI USB Interface Adapter PMBus pod (TI part number EVM USB-TO-GPIO), which can be ordered from the TI website [Ref 25], and the associated TI Fusion Digital Power Designer GUI (downloadable from [Ref 25]). This is the simplest and most convenient way to monitor the voltage and current values for the power rail listed in Table 1-30, Table 1-31, and Table 1-32.

In each of these the three tables (one per controller), the Power Good (PG) On Threshold is the set-point at or above which the particular rail is deemed "good". The PG Off Threshold is the set-point at or below which the particular rail is no longer deemed "good". The controller internally OR's these PG conditions together and drives an output PG pin high only if all active rail PG states are "good". The On and Off Delay and rise and fall times are relative to when the board power on-off slide switch SW12 is turned on and off.

产品种类:	FPGA - 现场可编程门阵列	☑
产品:	Virtex-II Pro	☐
系列:	XC2VP2	☐
逻辑元件数量:	3168 LE	☐
自适应逻辑模块 - ALM:	1408 ALM	☐
嵌入式内存:	216 kbit	☐
输入/输出端数量:	156 I/O	☐
工作电源电压:	1.5 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 85 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-456	☐
数据速率:	4.25 Gb/s	
商标:	Xilinx	
分布式RAM:	44 kbit	
内嵌式块RAM - EBR:	216 kbit	
最大工作频率:	300 MHz	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	352 LAB	
收发器数量:	4 Transceiver	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	60	
子类别:	Programmable Logic ICs	
商标名:	Virtex	

XC3330A-PC44I	2001+	PLCC-44	2315
XC3330A-PC44C-5400	2001+	PLCC-44	2315
XC3330A-PC44C	2001+	PLCC	2315
XC3330APC44-5030	2001+	PLCC	2315
XC3330APC44	2001+	PLCC	2315
XC3330A-7PC44I	2001+	PLCC44	2315
XC3330A-5C/PC44	2001+	PLCC	2315
XC3330A-2VQ64C5516	2001+	BGA	2315
XC3330A	2001+	PLCC	2315
XC3330-5TQ100C	2001+	QFP	2315
XC3330-5042PC68C	2001+	PLCC	2315
XC3330-5030PC44C	2001+	PLCC44	2315
XC3330-5003PC68C	2001+	PLCC68	2315
XC3330-50/PC44	2001+	PLCC	2315
XC3330	2001+	PLCC-44	2315
XC331000-4FT256I	2001+	BGA	2315
XC3256XL-10TQ144I	2001+	QFP	2315
XC3256XL-10TQ144C	2001+	BGA	2315
XC3256XL-10PQ208C	2001+	QFP	2315
XC3256XL-10FT256C	2001+	QFP	2315
XC3256XCTQ144	2001+	QFP	2315
XC3256TQ144APN-12C	2001+	QFP144	2315
XC3220	2001+	PLCC84	2315
XC3200A-4FG256G	2001+	BGA	2315
XC3195TMPQ208-3	2001+	QFP	2315
XC3195TM-5PC84	2001+	PLCC	2315
XC3195TM-4PP175C	2001+	PGA	2315
XC3195TM-4	2001+	N A	2315
XC3195TM-3PP175C	2001+	PGA	2315
XC3195TM-3PC84	2001+	PLCC	2315
XC3195TM-3	2001+	PLCC	2315
XC3195TM-1PQ208AKJ	2001+	QFP-208	2315
XC3195PQ208C-3	2001+	QFP	2315
XC3195PP175C	2001+	QFP	2315
XC3195ATMPQ160-3C	2001+	QFP	2315
XC3195ATM-4PP175C	2001+	PBGA	2315
XC3195ATM-3PP175C	2001+	PGA	2315
XC3195ATM-3 PQ208C	2001+	QFP	2315
XC3195ATM-3	2001+	PLCC	2315
XC3195ATM-2PC84	2001+	PLCC	2315
XC3195ATM	2001+	PLCC84	2315