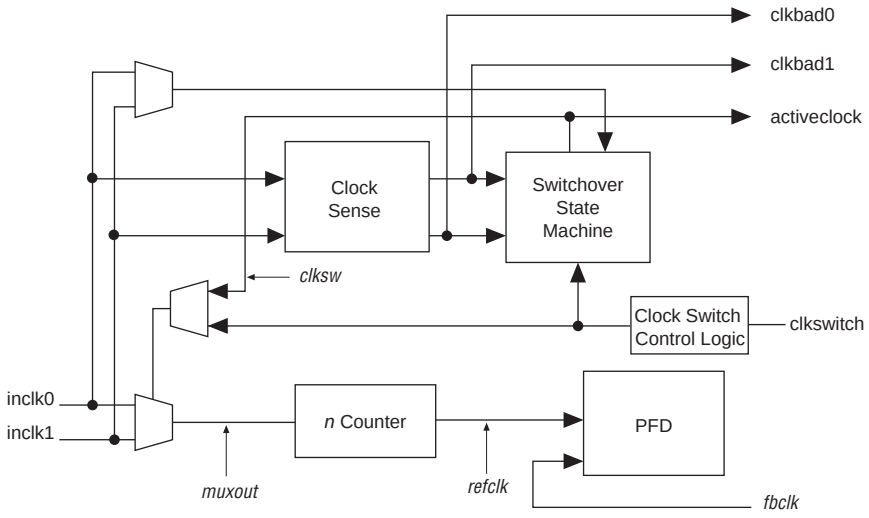
The following clock switchover modes are supported in Stratix III PLLs:

- Automatic switchover—The clock sense circuit monitors the current reference clock and if it stops toggling, automatically switches to the other clock `inclk0` or `inclk1`.
- Manual clock switchover—Clock switchover is controlled via the `clkswitch` signal in this mode. When the `clkswitch` signal goes from logic low to logic high, and stays high for at least three clock cycles, the reference clock to the PLL is switched from `inclk0` to `inclk1`, or vice-versa.
- Automatic switchover with manual override—This mode combines Modes 1 and 2. When the `clkswitch` signal goes high, it overrides automatic clock switchover mode.

Stratix III device PLLs support a fully configurable clock switchover capability. Figure 6–32 shows the block diagram of the switchover circuit built into the PLL. When the current reference clock is not present, the clock sense block automatically switches to the backup clock for PLL reference. The clock switchover circuit also sends out three status signals—`clkbad[0]`, `clkbad[1]`, and `activeclock`—from the PLL to implement a custom switchover circuit in the logic array. You can select a clock source as the backup clock by connecting it to the `inclk1` port of the PLL in your design.

Figure 6–32. Automatic Clock Switchover Circuit Block Diagram



Automatic Clock Switchover

Use the switchover circuitry to automatically switch between `inclk0` and `inclk1` when the current reference clock to the PLL stops toggling. For example, in applications that require a redundant clock with the same frequency as the reference clock, the switchover state machine generates a signal (`clksw`) that controls the multiplexer select input as shown in Figure 6–32. In this case, `inclk1` becomes the reference clock for the PLL. When using the automatic switchover mode, you can switch back and forth between `inclk0` and `inclk1` clocks any number of times, when one of the two clocks fails and the other clock is available.

When using the automatic clock switchover mode, the following requirements must be satisfied:

- Both clock inputs must be running.
- The period of the two clock inputs can differ by no more than 100% (2×).

If the current clock input stops toggling while the other clock is also not toggling, switchover will not be initiated and the `clkbad[0..1]` signals will not be valid. Also, if both clock inputs are not the same frequency, but their period difference is within 100%, the clock sense block will detect when a clock stops toggling, but the PLL may lose lock after the switchover is completed and need time to re-lock.

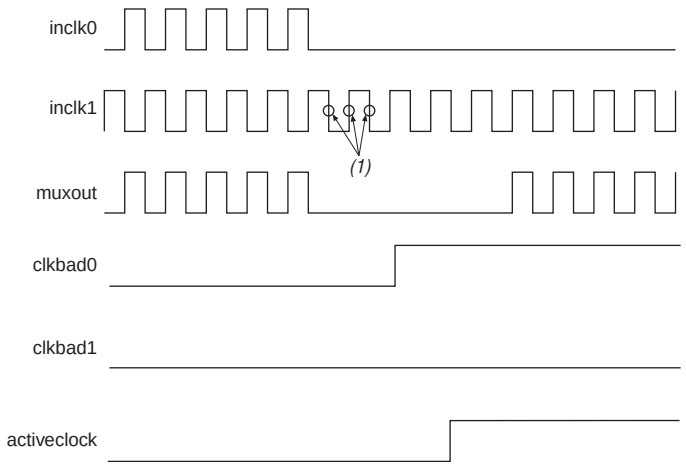
Altera recommends resetting the PLL using the `areset` signal to maintain the phase relationships between the PLL input and output clocks when using clock switchover.

When using automatic switchover mode, the `clkbad[0]` and `clkbad[1]` signals indicate the status of the two clock inputs. When they are asserted, the clock sense block has detected that the corresponding clock input has stopped toggling. These two signals are not valid if the frequency difference between `inclk0` and `inclk1` is greater than 20%.

The `activeclock` signal indicates which of the two clock inputs (`inclk0` or `inclk1`) is being selected as the reference clock to the PLL. When the frequency difference between the two clock inputs is more than 20%, the `activeclock` signal is the only valid status signal.

Figure 6–33 shows an example waveform of the switchover feature when using the automatic switchover mode. In this example, the `inclk0` signal remains low. After the `inclk0` signal remains low for approximately two clock cycles, the clock sense circuitry drives the `clkbad[0]` signal high. Also, because the reference clock signal is not toggling, the switchover state machine controls the multiplexer through the `clksw` signal to switch to the backup clock, `inclk1`.

Figure 6–33. Automatic Switchover Upon Loss of Clock Detection



Note to Figure 6–33:

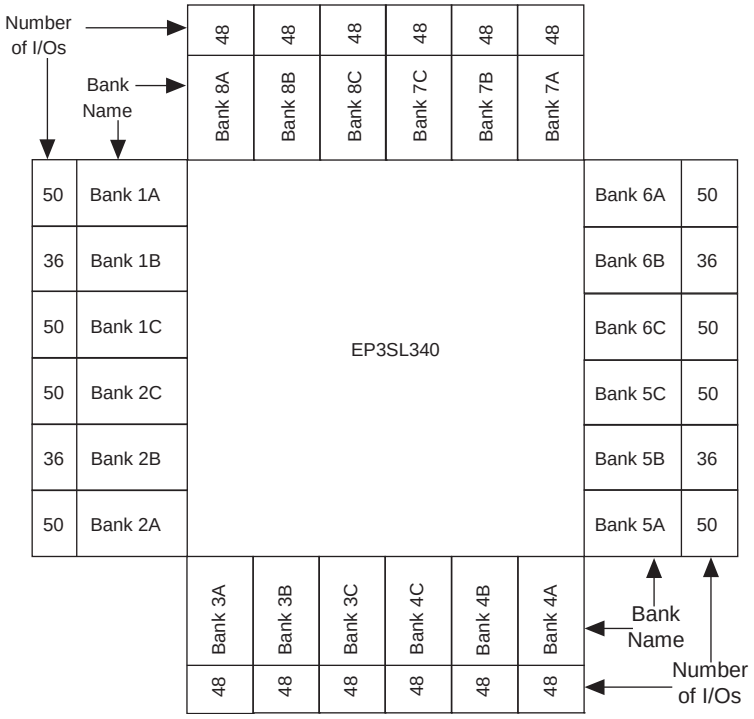
(1) Switchover is enabled on the falling edge of `inclk0` or `inclk1`, depending on which clock is available. In this figure, switchover is enabled on the falling edge of `inclk1`.

芯片详细信息

Manufacturer Part Number: EP2S180F1020C4	Rohs Code: No	Part Life Cycle Code: Not Recommended	Ihs Manufacturer: INTEL CORP
Package Description: 33 X 33 MM, 1 MM PITCH, FBGA-1020	Reach Compliance Code: compliant	ECCN Code: 3A001.A.7.A	HTS Code: 8542.39.00.01
Manufacturer: Intel Corporation	Risk Rank: 5.26	Clock Frequency-Max: 717 MHz	Combinatorial Delay of a CLB-Max: 5.117 ns
JESD-30 Code: S-PBGA-B1020	JESD-609 Code: e0	Length: 33 mm	Moisture Sensitivity Level: 4
Number of CLBs: 71760	Number of Inputs: 742	Number of Logic Cells: 179400	Number of Outputs: 734
Number of Terminals: 1020	Operating Temperature-Max: 85 °C	Organization: 71760 CLBS	Package Body Material: PLASTIC/EPOXY
Package Code: BGA	Package Equivalence Code: BGA1020,32X32,40	Package Shape: SQUARE	Package Style: GRID ARRAY
Peak Reflow Temperature (Cel): 220	Power Supplies: 1.2,1.5/3.3,3.3 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified
Seated Height-Max: 3.5 mm	Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V
Supply Voltage-Nom: 1.2 V	Surface Mount: YES	Technology: CMOS	Temperature Grade: OTHER
Terminal Finish: TIN LEAD	Terminal Form: BALL	Terminal Pitch: 1 mm	Terminal Position: BOTTOM
Time@Peak Reflow Temperature-Max (s): 30	Width: 33 mm		

RoHS:	N	
产品:	Stratix II	☐
系列:	Stratix II EP2S180	☐
逻辑元件数量:	179400 LE	☐
自适应逻辑模块 - ALM:	71760 ALM	☐
嵌入式内存:	8.95 Mbit	☐
输入/输出端数量:	742 I/O	☐
工作电源电压:	1.2 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 70 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-1020	☐
封装:	Tray	☐
商标:	Intel / Altera	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	8970 LAB	
工作电源电流:	1.12 A	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	24	
子类别:	Programmable Logic ICs	
总内存:	9383040 bit	
商标名:	Stratix II	
零件号别名:	970073	

Figure 7–6. Number of I/Os in Each Bank in EP3SL340 Devices in the 1760-pin FineLine BGA Package *(Note 1)*, *(2)*



Notes to Figure 7–6:

(1) All I/O pin counts include dedicated clock inputs pins. The pin count includes all general purpose I/O, dedicated clock pins, and dual-purpose configuration pins. Dedicated configuration pins are not included in the pin count.

(2) Figure 7–6 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

Stratix III I/O Structure

The I/O element (IOE) in Stratix III devices contains a bi-directional I/O buffer and I/O registers to support a complete embedded bi-directional single data rate or DDR transfer. The IOEs are located in I/O blocks around the periphery of the Stratix III device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row IOEs drive row, column, or direct link interconnects. The column IOEs drive column interconnects.

The Stratix III bi-directional IOE also supports the following features:

- Programmable input delay
- Programmable output-current strength
- Programmable slew rate
- Programmable output delay
- Programmable bus-hold
- Programmable pull-up resistor
- Open-drain output
- On-chip series termination with calibration