Stratix III devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Stratix III devices. During configuration, the Stratix III device decompresses the bitstream in real time and programs its SRAM cells.

Stratix III devices support decompression in the FPP when using a MAX II device/microprocessor plus flash, fast AS, and PS configuration schemes. The Stratix III decompression feature is not available in the FPP when using the enhanced configuration device and JTAG configuration schemes.

For more information, refer to the *Configuring Stratix III Devices* chapter.

Remote System Upgrades

Stratix III devices feature remote system upgrade capability, allowing error-free deployment of system upgrades from a remote location securely and reliably. Soft logic (either the Nios embedded processor or user logic) implemented in a Stratix III device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, and can recover from an error condition by reverting back to a safe configuration image, and provides error status information. This dedicated remote system upgrade circuitry is unique to Stratix series FPGAs and helps to avoid system downtime.

For more information, refer to the *Remote System Upgrades with Stratix III Devices* chapter.

IEEE 1149.1 (JTAG) Boundary-Scan Testing

Stratix III devices support the JTAG IEEE Std. 1149.1 specification. The Boundary-Scan Test (BST) architecture offers the capability to test pin connections without using physical test probes and capture functional data while a device is operating normally. Boundary-scan cells in the Stratix III device can force signals onto pins or capture data from pin or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. In addition to BST, you can use the IEEE Std. 1149.1 controller for Stratix III device in-circuit reconfiguration (ICR).

For more information, refer to the *IEEE 1149.1 (JTAG) Boundary Scan Testing in Stratix III Devices* chapter.

Design Security

Stratix III devices are high-density, high-performance FPGAs with support for 256-bit volatile and non-volatile security keys to protect designs against copying, reverse engineering, and tampering. Stratix III devices have the ability to decrypt a configuration bitstream using the Advanced Encryption Standard (AES) algorithm, an industry standard encryption algorithm that is FIPS-197 certified and requires a 256-bit security key.

The design security feature is available when configuring Stratix III FPGAs using the fast passive parallel (FPP) configuration mode with an external host (such as a MAX II device or microprocessor), or when using fast active serial (AS) or passive serial (PS) configuration schemes.

For more information about the design security feature, refer to the *Design Security in Stratix III Devices* chapter.

SEU Mitigation

Stratix III devices have built-in error detection circuitry to detect data corruption due to soft errors in the configuration random-access memory (CRAM) cells. This feature allows all CRAM contents to be read and verified continuously during user mode operation to match a configuration-computed CRC value. The enhanced CRC circuit and frame-based configuration architecture allows detection and location of multiple, single, and adjacent bit errors which, in conjunction with a soft circuit supplied as a reference design, allows don't-care soft errors in the CRAM to be ignored during device operation. This provides a steep decrease in the effective soft error rate, increasing system reliability.

On-chip memory block SEU mitigation is also offered using the ninth bit and a configurable megafunction in the Quartus II software for MLAB and M9K blocks while the M144K memory blocks have built-in error correction code (ECC) circuitry.

For more information about the dedicated error detection circuitry, refer to the *SEU Mitigation in Stratix III Devices* chapter.

Programmable Power

Stratix III delivers Programmable Power, the only FPGA with user programmable power options balancing today's power and performance requirements. Stratix III devices utilize the most advanced power-saving techniques, including a variety of process, circuit, and architecture optimizations and innovations. In addition, user controllable power reduction techniques provide an optimal balance of performance and power reduction specific for each design configured into the Stratix III FPGA. The Quartus II software (starting from version 6.1) automatically optimizes designs to meet the performance goals while simultaneously leveraging the programmable power-saving options available in the Stratix III FPGA without the need for any changes to the design flow.

For more information about Programmable Power in Stratix III devices, refer to the following documents:

- *Programmable Power and Temperature Sensing Diode in Stratix III Devices* chapter
- *AN 437: Power Optimization in Stratix III FPGAs*
- *Stratix III Programmable Power White Paper*

EP2S90F1020C3	122	BGA	20+	ALTERA
EP2S90F1020C3N	120	FBGA	20+	ALTERA
EP2S90F1020C4	120	FBGA	20+	ALTERA
EP2S90F1020C4N	300	FBGA	20+	ALTERA
EP2S90F1020C4N	300	BGA	20+	ALTERA
EP2S90F1020C5N	368	FCBGA1156	20+	ALTERA
EP2S90F1020I3N	482	BGA	20+	ALTERA
EP2S90F1020I4N	897	BGA	20+	ALTERA
EP2S90F1020I4N	50	BGA	20+	ALTERA/INTER
EP2S90F1020I4N	283	FCBGA901	20+	ALTERA
EP2S90F1508C5N	448	BGA	20+	ALTERA
EP2SGX130GF1508C3N	6	BGA	20+	Intel/Altera
EP2SGX130GF1508C3N	109	FCBGA900	20+	ALTERA
EP2SGX130GF1508C4N	80	BGA	20+	ALTERA
EP2SGX130GF1508C5N	488	BGA	20+	ALTERA
EP2SGX130GF1508I4N	47	BGA	20+	Intel/Altera
EP2SGX130GF1508I4N	280	BGA	20+	ALTERA
EP2SGX30DF780I4N	63	FBGA1761	20+	ALTERA
EP2SGX60CF780I4	69	BGA	20+	ALTERA
EP2SGX60EF1152C3N	163	BGA	20+	ALTERA
EP2SGX60EF1152C3N	50	BGA	20+	Intel/Altera
EP2SGX60EF1152C4N	120	BGA	20+	ALTERA
EP2SGX60EF1152C4N	57	BGA	20+	Intel/Altera
EP2SGX60EF1152C5N	200	BGA	20+	ALTERA
EP2SGX60EF1152I3N	120	BGA	20+	ALTERA
EP2SGX60EF1152I4N	347	FCBGA900	20+	ALTERA
EP2SGX90EF1152C3N	186	BGA	20+	ALTERA
EP2SGX90EF1152C3N	33	BGA	20+	Intel/Altera
EP2SGX90EF1152C4N	212	BGA	20+	ALTERA
EP2SGX90EF1152C4N	1000	BGA	20+	ALTERA
EP2SGX90EF1152I4N	16	BGA	20+	Intel/Altera
EP2SGX90EF1152I4N	98	FCBGA1158	20+	ALTERA
EP2SGX90FF1508C3N	10	BGA	20+	ALTERA
EP3SE110F1152C2N	88	BGA	20+	ALTERA
EP3SE110F1152C4N	100	BGA	20+	ALTERA
EP3SE110F1152I3N	1036	BGA	20+	ALTERA
EP3SE110F1152I3N	125	FCBGA1158	20+	ALTERA

SIII51002-1.5

EP3SE260F1152C2N	143	BGA	20+	ALTERA
EP3SE260F1152C4N	56	BGA	20+	ALTERA
EP3SE260F1152I3N	103	FCBGA1517	20+	ALTERA
EP3SE260F1152I4N	11335	SOT-23	20+	ALTERA
EP3SE260F1517C4N	120	BGA	20+	ALTERA
EP3SE260H780C4N	168	BGA	20+	ALTERA
EP3SE50F780C2N	473	BGA	20+	ALTERA
EP3SE50F780C3N	50	BGA	20+	ALTERA
EP3SE50F780C4N	10	BGA	20+	ALTERA
EP3SE50F780I3N	368	FCBGA1148	20+	ALTERA
EP3SE50F780I4N	178	FCBGA665	20+	ALTERA
EP3SE80F1152I3N	2	BGA	20+	Intel/Altera
EP3SE80F1152I4N	136	BGA	20+	ALTERA
EP3SE80F1152I4N	3	BGA	20+	Intel/Altera
EP3SE80F780C3N	466	BGA	20+	ALTERA
EP3SE80F780I3N	151	BGA	20+	ALTERA
EP3SL110F1152C2N	100	BGA	20+	ALTERA
EP3SL110F1152I3N	166	FCBGA1759	20+	ALTERA
EP3SL110F780C2N	168	FCBGA2104	20+	ALTERA
EP3SL110F780C3N	57	BGA	20+	Intel/Altera
EP3SL110F780C4N	156	BGA	20+	ALTERA
EP3SL110F780I3LN	50	BGA	20+	ALTERA
EP3SL110F780I3N	120	BGA	20+	ALTERA
EP3SL110F780I4LN	25	BGA	20+	ALTERA
EP3SL110F780I4N	6	BGA	20+	Intel/Altera
EP3SL110F780I4N	280	BGA	20+	ALTERA
EP3SL150F1152C4N	5	BGA	20+	Intel/Altera
EP3SL150F1152C4N	163	FBGA900	20+	ALTERA
EP3SL150F1152C4N	1000	BGA	20+	ALTERA
EP3SL150F1152I3N	300	BGA	20+	ALTERA
EP3SL150F1152I4N	500	BGA	20+	ALTERA
EP3SL150F780C2N	152	BGA	20+	ALTERA
EP3SL150F780I3N	1010	SOP	20+	ALTERA
EP3SL200F1152I3N	228	BGA	20+	ALTERA
EP3SL200F1152I4N	105	FBGA676	20+	ALTERA
EP3SL200F1517C3N	70	BGA	20+	ALTERA
EP3SL200H28I3N	50	BGA	20+	XILINX

C12 column interconnects span a length of 12 LABs and provide the fastest resource for column connections between distant LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C12 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly.

All embedded blocks communicate with the logic array through interconnects similar to LAB-to-LAB interfaces. Each block (for example, TriMatrix memory blocks and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB.

Table 3–1 shows the Stratix III device's routing scheme.

Table 3–1. Stratix III Device Routing Scheme

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R20 Interconnect	C4 Interconnect	C12 Interconnect	ALM	MLAB RAM Block	M9K RAM Block	M144K Block	DSP Blocks	Column IOE	Row IOE
Shared arithmetic chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Carry chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Register chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Local interconnect	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
Direct link interconnect	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—
R4 interconnect	—	—	—	✓	—	✓	✓	✓	✓	—	—	—	—	—	—	—
R20 interconnect	—	—	—	✓	—	✓	✓	✓	✓	—	—	—	—	—	—	—
C4 interconnect	—	—	—	✓	—	✓	—	✓	—	—	—	—	—	—	—	—
C12 interconnect	—	—	—	✓	—	✓	✓	✓	✓	—	—	—	—	—	—	—
ALM	✓	✓	✓	✓	✓	✓	—	✓	—	—	—	—	—	—	—	—
MLAB RAM block	—	—	—	✓	✓	✓	—	✓	—	—	—	—	—	—	—	—
M9K RAM block	—	—	—	—	✓	✓	—	✓	—	—	—	—	—	—	—	—
M144K block	—	—	—	—	✓	✓	—	✓	—	—	—	—	—	—	—	—
DSP blocks	—	—	—	—	✓	✓	—	✓	—	—	—	—	—	—	—	—
Column IOE	—	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	—
Row IOE	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—	—

Notes to Table 3–1:

(1) Except column IOE local interconnects.
(2) Row IOE local interconnects.
(3) Column IOE local interconnects.