### DLL and DQS Logic Block Specifications

Table 1–32 describes the DLL frequency range specifications for Stratix III devices.

**Table 1–32.** Stratix III DLL Frequency Range Specifications

| Frequency Mode | Frequency Range (MHz) | | | | Available Phase Shift | Number of Delay Chains | DQS Delay Buffer Mode *(1)* |
|---|---|---|---|---|---|---|---|
| | C2 | C3, I3 | C4, I4 | C4L, I4L | | | |
| 0 | 90 – 150 | 90 – 140 | 90 – 120 | 90 – 120 | 22.5°, 45°, 67.5°, 90° | 16 | Low |
| 1 | 120 – 200 | 120 – 190 | 120 – 170 | 120 – 170 | 30°, 60°, 90°, 120° | 12 | Low |
| 2 | 150 – 240 | 150 – 230 | 150 – 200 | 150 – 200 | 36°, 72°, 108°, 144° | 10 | Low |
| 3 | 180 – 300 | 180 – 290 | 180 – 250 | 180 – 250 | 45°, 90°,135°, 180° | 8 | Low |
| 4 | 240 – 370 | 240 – 350 | 240 – 310 | 240 – 310 | 30°, 60°, 90°,120° | 12 | High |
| 5 | 290 – 450 | 290 – 420 | 290 – 370 | 290 – 370 | 36°, 72°, 108°, 144° | 10 | High |
| 6 | 360 – 560 | 360 – 530 | 360 – 460 | 360 – 460 | 45°, 90°, 135°, 180° | 8 | High |
| 7 | 470 – 740 | 470 – 700 | 470 – 610 | 470 – 610 | 60°, 120°, 180°, 240° | 6 | High |

**Note to Table 1–32:**

(1) Low indicates 6-bit DQS delay setting, high indicates 5-bit DQS delay setting.

Table 1–33 describes the average DQS phase offset delay per setting for Stratix III devices.

**Table 1–33.** Average DQS Phase Offset Delay per Setting *(Note 1)*, *(2)*, *(3)*

| Speed Grade | Min | Typ | Max | Unit |
|---|---|---|---|---|
| C2 | 7 | 10 | 13 | ps |
| C3, I3 | 7 | 11 | 15 | ps |
| C4, I4 | 7 | 11.5 | 16 | ps |
| C4L, I4L | 7 | 11.5 | 16 | ps |

**Notes to Table 1–33:**

(1) The valid settings for phase offset are -64 to +63 for frequency modes 0 to 3 and -32 to +31 for frequency modes 4 to 6.

(2) The typical value equals the average of the minimum and maximum values.

(3) The delay settings are linear with a cumulative delay variation of ±20ps for all speed grades. For example, when using a C2 speed grade and applying 10° phase offset settings to a 90° phase shift at 400 MHz, the expected minimum cumulative delay is [625 ps + (10*7 ps) - 20 ps] = 675 ps.

**Table 1–34.** Stratix III DQS Phase Shift Error Specification for DLL-Delayed Clock (tDQS_PSERR) *(Note 1)*

| Number of DQS Delay Buffer | C2 | C3, I3 | C4, C4L, I4, I4L | Unit |
|---|---|---|---|---|
| 1 | ±13 | ±14 | ±15 | ps |
| 2 | ±26 | ±28 | ±30 | ps |
| 3 | ±39 | ±42 | ±45 | ps |
| 4 | ±52 | ±56 | ±60 | ps |

**Note to Table 1–34:**

(1) This error specification is the absolute maximum and minimum error. For example, skew on 3 DQS delay buffer in a C2 speed grade is ±39ps.

**Table 1–35.** Stratix III Memory Output Clock Jitter Specification *(Note 1), (2),(3)*

| Parameter | Clock Network | Symbol | C2 | | C3, I3 | | C4, I4 | | C4L, I4L | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CCL}$ = 1.1V | | $V_{CCL}$ = 1.1V | | $V_{CCL}$ = 1.1V | | $V_{CCL}$ = 1.1V | | $V_{CCL}$ = 0.9V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Clock period jitter | Regional | tJIT(per) | –70 | 70 | –85 | 85 | –100 | 100 | –100 | 100 | –120 | 120 | ps |
| Cycle-to-cycle period jitter | Regional | tJIT(cc) | –150 | 150 | –170 | 170 | –190 | 190 | –190 | 190 | –230 | 230 | ps |
| Duty cycle jitter | Regional | tJIT(duty) | –80 | 80 | –90 | 90 | –100 | 100 | –100 | 100 | –140 | 140 | ps |
| Clock period jitter | Global | tJIT(per) | –105 | 105 | –128 | 128 | –150 | 150 | –150 | 150 | –180 | 180 | ps |
| Cycle-to-cycle period jitter | Global | tJIT(cc) | –225 | 225 | –255 | 255 | –285 | 285 | –285 | 285 | –340 | 340 | ps |
| Duty cycle jitter | Global | tJIT(duty) | –120 | 120 | –135 | 135 | –150 | 150 | –150 | 150 | –180 | 180 | ps |

**Notes to Table 1–35:**

(1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 standard.

(2) The clock jitter specification applies to memory output clock pins generated using differential signal-splitter & DDIO circuits clocked by a PLL output routed on a regional or global clock network as specified. Use of regional clock networks are recommended whenever possible.

(3) The memory output clock jitter stated in the table is applicable when an input jitter of 30ps is applied.

## OCT Calibration Block Specifications

Table 1–36 shows the on-chip termination calibration block specifications for Stratix III devices.

**Table 1–36.** On-Chip Termination Calibration Block Specification

| Symbol | Description | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| OCTUSRCLK | Clock required by OCT calibration blocks | — | — | 20 | MHz |
| $t_{OCTCAL}$ | Number of OCTUSRCLK clock cycles required for OCT Rs and Rt calibration | — | 1000 | — | cycles |
| $t_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for OCT code to shift out per OCT calibration block | — | 28 | — | cycles |
| $t_{RS\_RT}$ | Time required to dynamically switch from Rs to Rt | — | 2.5 | — | ns |

## DCD Specifications

Table 1–37 lists the worst case duty cycle distortion for Stratix III devices. Detailed information on duty cycle distortion will be published after characterization.

**Table 1–37.** Duty Cycle Distortion on Stratix III I/O Pins *(Note 1)*

| Symbol | C2 | | C3 | | C4 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | % |

**Note to Table 1–37:**

(1) DCD specification applies to clock outputs from PLLs, global clock tree, and IOE driving dedicated and general purpose I/O pins.

芯片详细信息

| | | | |
|---|---|---|---|
| Manufacturer Part Number:<br>EP2S15F672I4 | Rohs Code:<br>No | Part Life Cycle Code:<br>Not Recommended | Ihs Manufacturer:<br>INTEL CORP |
| Package Description:<br>35 X 35 MM, 1 MM PITCH, FBGA-672 | Reach Compliance Code:<br>compliant | ECCN Code:<br>3A991 | HTS Code:<br>8542.39.00.01 |
| Manufacturer:<br>Intel Corporation | Risk Rank:<br>5.25 | Clock Frequency-Max:<br>717 MHz | Combinatorial Delay of a CLB-Max:<br>5.117 ns |
| JESD-30 Code:<br>S-PBGA-B672 | JESD-609 Code:<br>e0 | Length:<br>35 mm | Moisture Sensitivity Level:<br>3 |
| Number of CLBs:<br>6240 | Number of Inputs:<br>366 | Number of Logic Cells:<br>15600 | Number of Outputs:<br>358 |
| Number of Terminals:<br>672 | Operating Temperature-Max:<br>100 °C | Operating Temperature-Min:<br>-40 °C | Organization:<br>6240 CLBS |
| Package Body Material:<br>PLASTIC/EPOXY | Package Code:<br>BGA | Package Equivalence Code:<br>BGA672,26X26,40 | Package Shape:<br>SQUARE |
| Package Style:<br>GRID ARRAY | Peak Reflow Temperature (Cel):<br>220 | Power Supplies:<br>1.2,1.5/3.3,3.3 V | Programmable Logic Type:<br>FIELD PROGRAMMABLE GATE ARRAY |
| Qualification Status:<br>Not Qualified | Seated Height-Max:<br>2.6 mm | Subcategory:<br>Field Programmable Gate Arrays | Supply Voltage-Max:<br>1.25 V |
| Supply Voltage-Min:<br>1.15 V | Supply Voltage-Nom:<br>1.2 V | Surface Mount:<br>YES | Technology:<br>CMOS |
| Temperature Grade:<br>INDUSTRIAL | Terminal Finish:<br>TIN LEAD | Terminal Form:<br>BALL | Terminal Pitch:<br>1.27 mm |
| Terminal Position:<br>BOTTOM | Time@Peak Reflow Temperature-Max (s):<br>30 | Width:<br>35 mm | |

**Table 1–84.** EP3SL200 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 0.9V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 0.9V | |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -1.235 | -1.266 | -1.892 | -1.883 | -2.166 | -2.089 | -2.510 | -2.028 | -2.186 | -2.089 | -2.510 | ns |
| | | $t_h$ | 1.370 | 1.419 | 2.130 | 2.128 | 2.431 | 2.339 | 2.764 | 2.280 | 2.463 | 2.339 | 2.764 | ns |
| | GCLK PLL | $t_{su}$ | 0.978 | 0.992 | 1.751 | 1.957 | 2.171 | 2.052 | 1.977 | 1.855 | 2.071 | 2.052 | 1.977 | ns |
| | | $t_h$ | -0.700 | -0.696 | -1.273 | -1.457 | -1.615 | -1.528 | -1.441 | -1.345 | -1.506 | -1.528 | -1.441 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -1.235 | -1.266 | -1.892 | -1.883 | -2.166 | -2.089 | -2.510 | -2.028 | -2.186 | -2.089 | -2.510 | ns |
| | | $t_h$ | 1.370 | 1.419 | 2.130 | 2.128 | 2.431 | 2.339 | 2.764 | 2.280 | 2.463 | 2.339 | 2.764 | ns |
| | GCLK PLL | $t_{su}$ | 0.978 | 0.992 | 1.751 | 1.957 | 2.171 | 2.052 | 1.977 | 1.855 | 2.071 | 2.052 | 1.977 | ns |
| | | $t_h$ | -0.700 | -0.696 | -1.273 | -1.457 | -1.615 | -1.528 | -1.441 | -1.345 | -1.506 | -1.528 | -1.441 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -1.226 | -1.255 | -1.876 | -1.893 | -2.152 | -2.074 | -2.497 | -2.014 | -2.177 | -2.074 | -2.497 | ns |
| | | $t_h$ | 1.361 | 1.408 | 2.113 | 2.137 | 2.415 | 2.323 | 2.747 | 2.264 | 2.451 | 2.323 | 2.747 | ns |
| | GCLK PLL | $t_{su}$ | 0.987 | 1.001 | 1.766 | 1.882 | 2.174 | 2.064 | 1.973 | 1.869 | 2.080 | 2.064 | 1.973 | ns |
| | | $t_h$ | -0.709 | -0.705 | -1.288 | -1.387 | -1.620 | -1.542 | -1.441 | -1.361 | -1.518 | -1.542 | -1.441 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -1.226 | -1.255 | -1.876 | -1.893 | -2.152 | -2.074 | -2.497 | -2.014 | -2.177 | -2.074 | -2.497 | ns |
| | | $t_h$ | 1.361 | 1.408 | 2.113 | 2.137 | 2.415 | 2.323 | 2.747 | 2.264 | 2.451 | 2.323 | 2.747 | ns |
| | GCLK PLL | $t_{su}$ | 0.987 | 1.001 | 1.766 | 1.882 | 2.174 | 2.064 | 1.973 | 1.869 | 2.080 | 2.064 | 1.973 | ns |
| | | $t_h$ | -0.709 | -0.705 | -1.288 | -1.387 | -1.620 | -1.542 | -1.441 | -1.361 | -1.518 | -1.542 | -1.441 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -1.212 | -1.243 | -1.863 | -1.883 | -2.134 | -2.056 | -2.479 | -2.003 | -2.160 | -2.056 | -2.479 | ns |
| | | $t_h$ | 1.347 | 1.396 | 2.101 | 2.127 | 2.397 | 2.305 | 2.729 | 2.253 | 2.434 | 2.305 | 2.729 | ns |
| | GCLK PLL | $t_{su}$ | 1.001 | 1.013 | 1.781 | 1.892 | 2.192 | 2.082 | 1.991 | 1.880 | 2.097 | 2.082 | 1.991 | ns |
| | | $t_h$ | -0.723 | -0.717 | -1.302 | -1.397 | -1.638 | -1.560 | -1.459 | -1.372 | -1.535 | -1.560 | -1.459 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -1.226 | -1.255 | -1.876 | -1.893 | -2.152 | -2.074 | -2.497 | -2.014 | -2.177 | -2.074 | -2.497 | ns |
| | | $t_h$ | 1.361 | 1.408 | 2.113 | 2.137 | 2.415 | 2.323 | 2.747 | 2.264 | 2.451 | 2.323 | 2.747 | ns |
| | GCLK PLL | $t_{su}$ | 0.987 | 1.001 | 1.766 | 1.882 | 2.174 | 2.064 | 1.973 | 1.869 | 2.080 | 2.064 | 1.973 | ns |
| | | $t_h$ | -0.709 | -0.705 | -1.288 | -1.387 | -1.620 | -1.542 | -1.441 | -1.361 | -1.518 | -1.542 | -1.441 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -1.226 | -1.255 | -1.876 | -1.893 | -2.152 | -2.074 | -2.497 | -2.014 | -2.177 | -2.074 | -2.497 | ns |
| | | $t_h$ | 1.361 | 1.408 | 2.113 | 2.137 | 2.415 | 2.323 | 2.747 | 2.264 | 2.451 | 2.323 | 2.747 | ns |
| | GCLK PLL | $t_{su}$ | 0.987 | 1.001 | 1.766 | 1.882 | 2.174 | 2.064 | 1.973 | 1.869 | 2.080 | 2.064 | 1.973 | ns |
| | | $t_h$ | -0.709 | -0.705 | -1.288 | -1.387 | -1.620 | -1.542 | -1.441 | -1.361 | -1.518 | -1.542 | -1.441 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -1.212 | -1.243 | -1.863 | -1.883 | -2.134 | -2.056 | -2.479 | -2.003 | -2.160 | -2.056 | -2.479 | ns |
| | | $t_h$ | 1.347 | 1.396 | 2.101 | 2.127 | 2.397 | 2.305 | 2.729 | 2.253 | 2.434 | 2.305 | 2.729 | ns |
| | GCLK PLL | $t_{su}$ | 1.001 | 1.013 | 1.781 | 1.892 | 2.192 | 2.082 | 1.991 | 1.880 | 2.097 | 2.082 | 1.991 | ns |
| | | $t_h$ | -0.723 | -0.717 | -1.302 | -1.397 | -1.638 | -1.560 | -1.459 | -1.372 | -1.535 | -1.560 | -1.459 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -1.212 | -1.243 | -1.863 | -1.883 | -2.134 | -2.056 | -2.479 | -2.003 | -2.160 | -2.056 | -2.479 | ns |
| | | $t_h$ | 1.347 | 1.396 | 2.101 | 2.127 | 2.397 | 2.305 | 2.729 | 2.253 | 2.434 | 2.305 | 2.729 | ns |
| | GCLK PLL | $t_{su}$ | 1.001 | 1.013 | 1.781 | 1.892 | 2.192 | 2.082 | 1.991 | 1.880 | 2.097 | 2.082 | 1.991 | ns |
| | | $t_h$ | -0.723 | -0.717 | -1.302 | -1.397 | -1.638 | -1.560 | -1.459 | -1.372 | -1.535 | -1.560 | -1.459 | ns |

| | | |
|---|---|---|
| 产品种类: | FPGA - 现场可编程门阵列 | ☑ |
| RoHS: | N | |
| 产品: | Stratix II | ☐ |
| 系列: | Stratix II EP2S15 | ☐ |
| 逻辑元件数量: | 15600 LE | ☐ |
| 自适应逻辑模块 - ALM: | 6240 ALM | ☐ |
| 嵌入式内存: | 409.5 kbit | ☐ |
| 输入/输出端数量: | 366 I/O | ☐ |
| 工作电源电压: | 1.2 V | ☐ |
| 最小工作温度: | - 40 C | ☐ |
| 最大工作温度: | + 85 C | ☐ |
| 安装风格: | SMD/SMT | ☐ |
| 封装 / 箱体: | FBGA-672 | ☐ |
| 封装: | Tray | ☐ |
| 商标: | Intel / Altera | |
| 湿度敏感性: | Yes | |
| 逻辑数组块数量——LAB: | 780 LAB | |
| 工作电源电流: | 250 mA | |
| 产品类型: | FPGA - Field Programmable Gate Array | |
| 工厂包装数量: | 40 | |
| 子类别: | Programmable Logic ICs | |
| 总内存: | 419328 bit | |
| 商标名: | Stratix II | |
| 零件号别名: | 974300 | |