DC Characteristics

This section lists the input pin capacitances, on-chip termination tolerance, and hot- socketing specifications.

Supply Current

Standby current is the current the device draws after the device is configured with no inputs/outputs toggling and no activity in the device. Since these currents vary largely with the resources used, use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design.

Table 1–4 lists supply current specifications for V_{CC_CLKIN} and V_{CCPGM}. Use the EPE to get supply current estimates for remaining power supplies.

Table 1–4. Supply Current Specifications for V_{CC_CLKIN} and V_{CCPGM}

Symbol	Parameter	Min	Max	Unit
I_{CLKIN}	V_{CC_CLKIN} current specifications	0	250	mA
I_{PGM}	V_{CCPGM} current specifications	0	250	mA

I/O Pin Leakage Current

Table 1–5 defines Stratix III I/O Pin leakage current specifications.

Table 1–5. Stratix III I/O Pin Leakage Current *(Note 1)*, *(2)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input Pin Leakage Current	$V_I = V_{CCIOMAX}$ to 0 V	-10	—	10	µA
I_{OZ}	Tri-stated I/O Pin Leakage Current	$V_O = V_{CCIOMAX}$ to 0 V	-10	—	10	µA

Notes to Table 1–5:

(1) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) 10-µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

Bus Hold Specifications

Table 1–7 shows the Stratix III device family bus hold specifications.

Table 1–6. Bus Hold Parameters (Part 1 of 2)

Parameter	Symbol	Conditions	V_{CCIO}										Unit
			1.2V		1.5V		1.8V		2.5V		3.0V/3.3V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I_{SUSL}	$V_{IN}>V_{IL}$ (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	µA
High sustaining current	I_{SUSH}	$V_{IN}<V_{IH}$ (minimum)	-22.5	—	-25.0	—	-30.0	—	-50.0	—	-70.0	—	µA
Low overdrive current	I_{ODL}	$0V<V_{IN}<V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA

Table 1–91 specifies EP3SL200 Column Pin delay adders when using the regional clock.

Table 1–91. EP3SL200 Column Pin Delay Adders for Regional Clock

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
RCLK input adder	0.204	0.235	0.378	0.378	0.403	0.392	0.509	0.387	0.411	0.392	0.509	ns
RCLK PLL input adder	0.036	0.046	0.078	0.078	-0.047	-0.038	-0.036	0.085	-0.046	-0.038	-0.036	ns
RCLK output adder	-0.211	-0.234	-0.332	-0.328	-0.34	-0.334	-0.464	-0.327	-0.339	-0.334	-0.464	ns
RCLK PLL output adder	1.904	1.965	3.193	3.323	3.688	3.496	3.804	3.351	3.716	3.496	3.804	ns

Table 1–92 specifies EP3SL200 Row Pin delay adders when using the regional clock.

Table 1–92. EP3SL200 Row Pin Delay Adders for Regional Clock

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
RCLK input adder	0.272	0.301	0.446	0.424	0.473	0.46	0.547	0.454	0.481	0.46	0.547	ns
RCLK PLL input adder	0.14	0.149	0.226	0.216	0.235	0.226	0.306	0.232	0.254	0.226	0.306	ns
RCLK output adder	-0.278	-0.306	-0.418	-0.434	-0.486	-0.472	-0.592	-0.464	-0.493	-0.472	-0.592	ns
RCLK PLL output adder	-0.15	-0.15	-0.227	-0.233	-0.254	-0.243	-0.322	-0.243	-0.258	-0.243	-0.322	ns

EP3SL340 I/O Timing Parameters

Table 1–93 through Table 1–96 show the maximum I/O timing parameters for EP3SL340 devices for single-ended I/O standards.

Table 1–93 specifies EP3SL340 column pins input timing parameters for single-ended I/O standards.

Table 1–93. EP3SL340 Column Pins Input Timing Parameters (Part 1 of 4)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.3-V LVTTL	GCLK	t_{su}	-1.469	-1.445	-2.196	-2.240	-2.531	-2.574	-2.974	-2.425	-2.680	-2.476	-3.011	ns
		t_h	1.600	1.594	2.424	2.477	2.791	2.819	3.231	2.670	2.949	2.735	3.269	ns
	GCLK PLL	t_{su}	0.630	0.633	1.173	1.252	1.305	1.231	1.218	1.246	1.315	1.198	1.271	ns
		t_h	-0.359	-0.343	-0.708	-0.768	-0.767	-0.728	-0.694	-0.751	-0.765	-0.680	-0.744	ns
3.3-V LVCMOS	GCLK	t_{su}	-1.469	-1.445	-2.196	-2.240	-2.531	-2.574	-2.974	-2.425	-2.680	-2.476	-3.011	ns
		t_h	1.600	1.594	2.424	2.477	2.791	2.819	3.231	2.670	2.949	2.735	3.269	ns
	GCLK PLL	t_{su}	0.630	0.633	1.173	1.252	1.305	1.231	1.218	1.246	1.315	1.198	1.271	ns
		t_h	-0.359	-0.343	-0.708	-0.768	-0.767	-0.728	-0.694	-0.751	-0.765	-0.680	-0.744	ns

Table 1–96. EP3SL340 Row Pins output Timing Parameters (Part 2 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8 V	2mA	GCLK	t_{co}	3.692	3.942	5.817	6.193	6.841	6.698	7.084	6.248	6.991	6.682	7.186	ns
		GCLK PLL	t_{co}	1.785	1.925	2.574	2.860	3.162	3.173	3.192	2.985	3.287	3.292	3.203	ns
	4mA	GCLK	t_{co}	3.519	3.756	5.527	5.824	6.436	6.293	6.679	5.922	6.585	6.320	6.779	ns
		GCLK PLL	t_{co}	1.562	1.739	2.284	2.491	2.757	2.768	2.787	2.620	2.881	2.885	2.796	ns
	6mA	GCLK	t_{co}	3.444	3.674	5.427	5.674	6.277	6.134	6.520	5.808	6.412	6.215	6.607	ns
		GCLK PLL	t_{co}	1.495	1.657	2.184	2.341	2.598	2.609	2.628	2.452	2.708	2.713	2.624	ns
	8mA	GCLK	t_{co}	3.426	3.654	5.370	5.595	6.180	6.037	6.423	5.752	6.318	6.143	6.513	ns
		GCLK PLL	t_{co}	1.469	1.637	2.127	2.259	2.501	2.512	2.531	2.361	2.614	2.619	2.530	ns
1.5 V	2mA	GCLK	t_{co}	3.634	3.885	5.745	6.106	6.769	6.626	7.012	6.169	6.915	6.617	7.110	ns
		GCLK PLL	t_{co}	1.696	1.868	2.502	2.773	3.090	3.101	3.120	2.892	3.211	3.216	3.127	ns
	4mA	GCLK	t_{co}	3.442	3.671	5.423	5.669	6.278	6.135	6.521	5.805	6.411	6.216	6.606	ns
		GCLK PLL	t_{co}	1.485	1.654	2.180	2.336	2.599	2.610	2.629	2.446	2.707	2.712	2.623	ns
	6mA	GCLK	t_{co}	3.415	3.645	5.355	5.587	6.172	6.029	6.415	5.745	6.306	6.143	6.501	ns
		GCLK PLL	t_{co}	1.458	1.628	2.112	2.251	2.493	2.504	2.523	2.354	2.602	2.607	2.518	ns
	8mA	GCLK	t_{co}	3.396	3.634	5.338	5.562	6.153	6.010	6.396	5.721	6.284	6.124	6.479	ns
		GCLK PLL	t_{co}	1.439	1.617	2.095	2.226	2.474	2.485	2.504	2.330	2.580	2.585	2.496	ns
1.2 V	2mA	GCLK	t_{co}	3.564	3.798	5.666	6.020	6.694	6.551	6.937	6.100	6.831	6.548	7.026	ns
		GCLK PLL	t_{co}	1.639	1.781	2.423	2.687	3.015	3.026	3.045	2.804	3.127	3.132	3.043	ns
	4mA	GCLK	t_{co}	3.447	3.675	5.440	5.697	6.319	6.176	6.562	5.834	6.453	6.260	6.648	ns
		GCLK PLL	t_{co}	1.490	1.658	2.197	2.364	2.640	2.651	2.670	2.471	2.749	2.754	2.665	ns
SSTL-2 CLASS I	8mA	GCLK	t_{co}	3.328	3.591	5.278	5.474	6.038	5.895	6.281	5.602	6.165	5.985	6.360	ns
		GCLK PLL	t_{co}	1.411	1.575	2.039	2.150	2.359	2.370	2.378	2.247	2.461	2.466	2.389	ns
	12mA	GCLK	t_{co}	3.323	3.587	5.275	5.472	6.030	5.887	6.273	5.601	6.158	5.984	6.353	ns
		GCLK PLL	t_{co}	1.406	1.570	2.032	2.148	2.351	2.362	2.370	2.246	2.454	2.459	2.382	ns
SSTL-2 CLASS II	16mA	GCLK	t_{co}	3.314	3.576	5.260	5.456	6.003	5.860	6.246	5.584	6.131	5.966	6.326	ns
		GCLK PLL	t_{co}	1.397	1.559	2.017	2.132	2.324	2.335	2.343	2.229	2.427	2.432	2.355	ns

产品种类:	FPGA - 现场可编程门阵列	☑
RoHS:	RoHS 详细信息	
产品:	Stratix II	☐
系列:	Stratix II EP2S15	☐
逻辑元件数量:	15600 LE	☐
自适应逻辑模块 - ALM:	6240 ALM	☐
嵌入式内存:	409.5 kbit	☐
输入/输出端数量:	366 I/O	☐
工作电源电压:	1.2 V	☐
最小工作温度:	- 40 C	☐
最大工作温度:	+ 85 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-672	☐
封装:	Tray	☐
商标:	Intel / Altera	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	780 LAB	
工作电源电流:	250 mA	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	40	
子类别:	Programmable Logic ICs	
总内存:	419328 bit	
商标名:	Stratix II	
零件号别名:	973062	

芯片详细信息

Manufacturer Part Number: EP2S15F672I4N	Rohs Code: Yes	Part Life Cycle Code: Active	Ihs Manufacturer: INTEL CORP
Package Description: 27 X 27 MM, 1 MM PITCH, LEAD FREE, FBGA-672	Reach Compliance Code: compliant	ECCN Code: 3A991	HTS Code: 8542.39.00.01
Manufacturer: Intel Corporation	Risk Rank: 5.26	Clock Frequency-Max: 717 MHz	Combinatorial Delay of a CLB-Max: 5.117 ns
JESD-30 Code: S-PBGA-B672	JESD-609 Code: e1	Length: 27 mm	Moisture Sensitivity Level: 3
Number of CLBs: 780	Number of Inputs: 366	Number of Logic Cells: 15600	Number of Outputs: 358
Number of Terminals: 672	Operating Temperature-Max: 100 °C	Operating Temperature-Min: -40 °C	Organization: 780 CLBS
Package Body Material: PLASTIC/EPOXY	Package Code: BGA	Package Equivalence Code: BGA672,26X26,40	Package Shape: SQUARE
Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 245	Power Supplies: 1.2,1.5/3.3,3.3 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY
Qualification Status: Not Qualified	Seated Height-Max: 3.5 mm	Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V
Supply Voltage-Min: 1.15 V	Supply Voltage-Nom: 1.2 V	Surface Mount: YES	Technology: CMOS
Temperature Grade: INDUSTRIAL	Terminal Finish: Tin/Silver/Copper (Sn/Ag/Cu)	Terminal Form: BALL	Terminal Pitch: 1 mm
Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 40	Width: 27 mm	