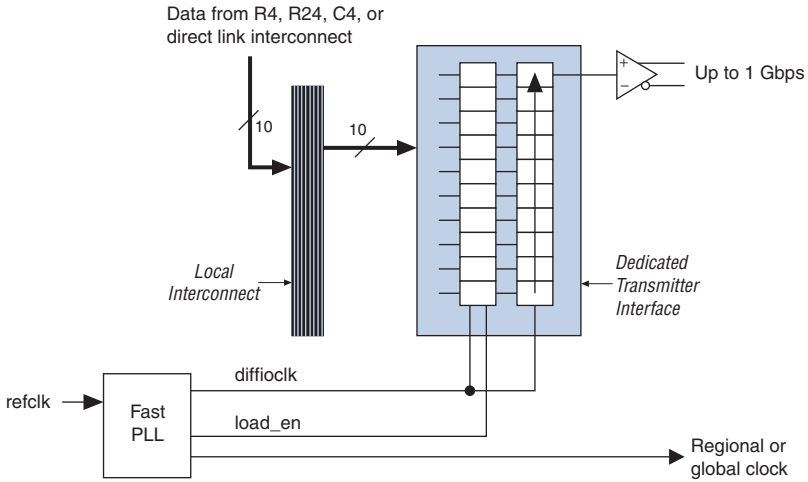
Dedicated Circuitry with DPA Support

Stratix II devices support source-synchronous interfacing with LVDS or HyperTransport signaling at up to 1 Gbps. Stratix II devices can transmit or receive serial channels along with a low-speed or high-speed clock. The receiving device PLL multiplies the clock by an integer factor W = 1 through 32. For example, a HyperTransport technology application where the data rate is 1,000 Mbps and the clock rate is 500 MHz would require that W be set to 2. The SERDES factor *J* determines the parallel data width to deserialize from receivers or to serialize for transmitters. The SERDES factor *J* can be set to 4, 5, 6, 7, 8, 9, or 10 and does not have to equal the PLL clock-multiplication W value. A design using the dynamic phase aligner also supports all of these *J* factor values. For a *J* factor of 1, the Stratix II device bypasses the SERDES block. For a *J* factor of 2, the Stratix II device bypasses the SERDES block, and the DDR input and output registers are used in the IOE. Figure 2–58 shows the block diagram of the Stratix II transmitter channel.

Figure 2–58. Stratix II Transmitter Channel



Each Stratix II receiver channel features a DPA block for phase detection and selection, a SERDES, a synchronizer, and a data realigner circuit. You can bypass the dynamic phase aligner without affecting the basic source-synchronous operation of the channel. In addition, you can dynamically switch between using the DPA block or bypassing the block via a control signal from the logic array. Figure 2–59 shows the block diagram of the Stratix II receiver channel.

EP1S25F672C7N	200	FBGA	20+	ALTERA
EP1S25F672I7	500	BGA	20+	ALTERA
EP1S25F780C7N	248	BGA1136	20+	ALTERA
EP1S25F780I6	42	BGA	20+	ALTERA
EP1S30F1020I6	168	BGA	20+	ALTERA
EP1S30F1020I6N	50	BGA	20+	ALTERA
EP1S30F780I6	172	BGA	20+	ALTERA
EP1S30F780I6N	195	FBGA676	20+	ALTERA
EP1S40B956I6	228	BGA	20+	ALTERA
EP1S40F1020I6	480	BGA	20+	ALTERA
EP1S40F780I6	240	BGA	20+	ALTERA
EP1S60B956I7	332	BGA	20+	ALTERA
EP1S60F1020C6N	56	FBGA1926	20+	ALTERA
EP1S60F1020C7N	20	FBGA1157	20+	ALTERA
EP1S80F1020C5N	143	BGA1759	20+	ALTERA
EP1S80F1020I6N	453	FCBGA1156	20+	ALTERA
EP1SGX25DF672C7N	20	BGA	20+	ALTERA
EP1SGX40DF1020C6N	386	BGA	20+	ALTERA
EP1SGX40GF1020I6	5	BGA	20+	ALTERA
EP2A15F672C7N	269	BGA1156	20+	ALTERA
EP2AGX125EF29C4N	300	BGA	20+	ALTERA
EP2AGX125EF29C4N	120	BGA	20+	Intel/Altera
EP2AGX125EF29C5N	215	BGA1517	20+	ALTERA
EP2AGX125EF29C6G	88	BGA	20+	ALTERA
EP2AGX125EF29I3N	680	BGA	20+	Intel/Altera
EP2AGX125EF29I3N	710	LSSN	20+	ALTERA
EP2AGX125EF35C5N	192	BGA	20+	ALTERA
EP2AGX125EF35I3N	280	BGA	20+	ALTERA
EP2AGX125EF35I5N	120	BGA	20+	ALTERA
EP2AGX190EF29C4N	130	BGA	20+	ALTERA
EP2AGX190EF29C5N	117	BGA	20+	ALTERA
EP2AGX190EF29C6G	172	BGA	20+	XILINX
EP2AGX190EF29C6N	461	BGA	20+	ALTERA
EP2AGX190EF29I3N	96	BGA	20+	ALTERA
EP2AGX190EF29I5N	55	BGA	20+	Intel/Altera
EP2AGX190FF35C5N	500	BGA	20+	ALTERA
EP2AGX190FF35C6N	30	BGA	20+	ALTERA

you need to support configuration input voltages of 1.8 V/1.5 V, you should set the VCCSEL to a logic high and the V_{CCIO} of the bank that contains the configuration inputs to 1.8 V/1.5 V.

For more information on multi-volt support, including information on using TDO and nCEO in multi-volt systems, refer to the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Configuration Schemes

You can load the configuration data for a Stratix II device with one of five configuration schemes (see Table 3–5), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix II device. A configuration device can automatically configure a Stratix II device at system power-up.

You can configure multiple Stratix II devices in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Stratix II FPGAs offer the following:

- Configuration data decompression to reduce configuration file storage
- Design security using configuration data encryption to protect your designs
- Remote system upgrades for remotely updating your Stratix II designs

Table 3–5 summarizes which configuration features can be used in each configuration scheme.

Table 3–5. Stratix II Configuration Features (Part 1 of 2)

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
FPP	MAX II device or microprocessor and flash device	✓ *(1)*	✓ *(1)*	✓
	Enhanced configuration device		✓ *(2)*	✓
AS	Serial configuration device	✓	✓	✓ *(3)*
PS	MAX II device or microprocessor and flash device	✓	✓	✓
	Enhanced configuration device	✓	✓	✓
	Download cable *(4)*	✓	✓	

EP2AGX190FF35C6N	30	BGA	20+	ALTERA
EP2AGX190FF35I3N	400	FBGA665	20+	ALTERA
EP2AGX190FF35I5N	1080	TQFP	20+	ALTERA
EP2AGX260EF29C5N	12	BGA	20+	ALTERA
EP2AGX260EF29C6N	25	BGA	20+	Intel/Altera
EP2AGX260EF29I3N	25	BGA	20+	Intel/Altera
EP2AGX260FF35C4N	2000	SOP	20+	ALTERA
EP2AGX260FF35C6N	110	FBGA	20+	ALTERA
EP2AGX260FF35I3N	263	FCBGA676	20+	ALTERA
EP2AGX260FF35I5N	165	BGA	20+	ALTERA
EP2AGX45CU17C4N	50	BGA	20+	ALTERA
EP2AGX45CU17I3G	50	BGA	20+	ALTERA
EP2AGX45DF25I3N	100	FBGA1156	20+	ALTERA
EP2AGX45DF29C5N	293	FCBGA1152	20+	ALTERA
EP2AGX45DF29I3N	167	FBGA1156	20+	ALTERA
EP2AGX65DF25C6N	263	FCBGA1738	20+	ALTERA
EP2AGX65DF25I3N	500	BGA900	20+	ALTERA
EP2AGX65DF25I5N	190	BGA2397	20+	XILINX
EP2AGX65DF25I5N	120	FBGA	20+	ALTERA
EP2AGX65DF29C4N	120	FBGA	20+	ALTERA
EP2AGX65DF29C5N	45	BGA	20+	ALTERA
EP2AGX65DF29C6N	116	FCBGA1517	20+	ALTERA
EP2AGX65DF29I3N	60	BGA	20+	Intel/Altera
EP2AGX65DF29I3N	133	FCBGA1517	20+	ALTERA
EP2AGX65DF29I5N	172	BGA	20+	ALTERA
EP2AGX95DF25C4N	200	FCBGA	20+	ALTERA
EP2AGX95DF25C6N	160	FCBGA	20+	ALTERA
EP2AGX95DF25I3	160	FCBGA	20+	ALTERA
EP2AGX95DF25I3N	160	FCBGA	20+	ALTERA
EP2AGX95DF25I5N	58	FPBGA1020	20+	ALTERA
EP2AGX95EF29C4N	1080	BGA	20+	ALTERA
EP2AGX95EF29C5N	50	BGA	20+	Intel/Altera
EP2AGX95EF29C5N	50	BGA	20+	ALTERA
EP2AGX95EF29C6N	15	BGA	20+	ALTERA
EP2AGX95EF29I3N	72	FBGA1156	20+	ALTERA
EP2AGX95EF35C6N	455	FBGA1152	20+	ALTERA
EP2AGX95EF35I3N	400	DIP	20+	ALTERA

Table 5–5. LVTTL Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(2)*		0.45	V

Notes to Tables 5–5:

(1) Stratix II devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–6. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		3.135	3.465	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA *(2)*	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA *(2)*		0.2	V

Notes to Table 5–6:

(1) Stratix II devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–7. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –1mA *(2)*	2.0		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA *(2)*		0.4	V

Notes to Table 5–7:

(1) Stratix II devices V_{CCIO} voltage level support of 2.5 ± -5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.