you need to support configuration input voltages of 1.8 V/1.5 V, you should set the VCCSEL to a logic high and the V_{CCIO} of the bank that contains the configuration inputs to 1.8 V/1.5 V.

For more information on multi-volt support, including information on using TDO and nCEO in multi-volt systems, refer to the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Configuration Schemes

You can load the configuration data for a Stratix II device with one of five configuration schemes (see Table 3–5), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix II device. A configuration device can automatically configure a Stratix II device at system power-up.

You can configure multiple Stratix II devices in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Stratix II FPGAs offer the following:

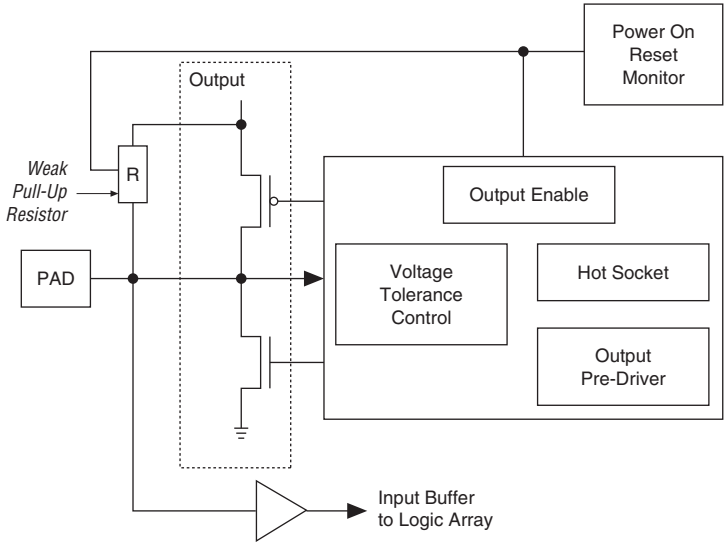
- Configuration data decompression to reduce configuration file storage
- Design security using configuration data encryption to protect your designs
- Remote system upgrades for remotely updating your Stratix II designs

Table 3–5 summarizes which configuration features can be used in each configuration scheme.

Table 3–5. Stratix II Configuration Features (Part 1 of 2)

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
FPP	MAX II device or microprocessor and flash device	✓ *(1)*	✓ *(1)*	✓
	Enhanced configuration device		✓ *(2)*	✓
AS	Serial configuration device	✓	✓	✓ *(3)*
PS	MAX II device or microprocessor and flash device	✓	✓	✓
	Enhanced configuration device	✓	✓	✓
	Download cable *(4)*	✓	✓	

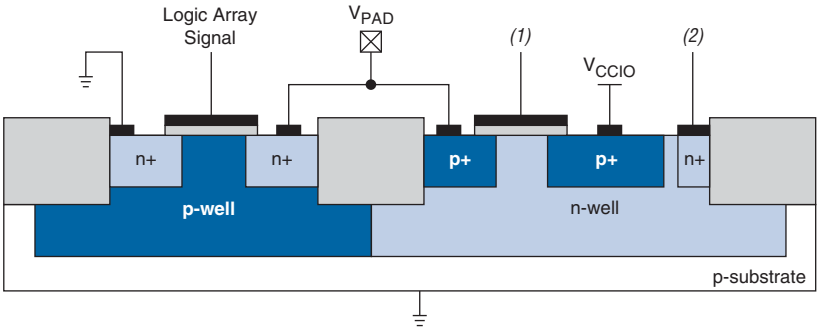
Figure 4–1. Hot Socketing Circuit Block Diagram for Stratix II Devices



The POR circuit monitors V_{CCINT} voltage level and keeps I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} is present to keep the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} and/or V_{CCPD} are powered, and it prevents the I/O pins from driving out when the device is not in user mode. The hot socket circuit prevents I/O pins from internally powering V_{CCIO}, V_{CCINT}, and V_{CCPD} when driven by external signals before the device is powered.

Figure 4–2 shows a transistor level cross section of the Stratix II device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot insertion. There is no current path from signal I/O pins to V_{CCINT} or V_{CCIO} or V_{CCPD} during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

Figure 4–2. Transistor Level Diagram of FPGA Device I/O Buffers



Notes to Figure 4–2:

(1) This is the logic array signal or the larger of either the V_{CCIO} or V_{PAD} signal.

(2) This is the larger of either the V_{CCIO} or V_{PAD} signal.

Power-On Reset Circuitry

Stratix II devices have a POR circuit to keep the whole device system in reset state until the power supply voltage levels have stabilized during power-up. The POR circuit monitors the V_{CCINT}, V_{CCIO}, and V_{CCPD} voltage levels and tri-states all the user I/O pins while V_{CC} is ramping up until normal user levels are reached. The POR circuitry also ensures that all eight I/O bank V_{CCIO} voltages, V_{CCPD} voltage, as well as the logic array V_{CCINT} voltage, reach an acceptable level before configuration is triggered. After the Stratix II device enters user mode, the POR circuit continues to monitor the V_{CCINT} voltage level so that a brown-out condition during user mode can be detected. If there is a V_{CCINT} voltage sag below the Stratix II operational level during user mode, the POR circuit resets the device.

When power is applied to a Stratix II device, a power-on-reset event occurs if V_{CC} reaches the recommended operating range within a certain period of time (specified as a maximum V_{CC} rise time). The maximum V_{CC} rise time for Stratix II device is 100 ms. Stratix II devices provide a dedicated input pin (PORSEL) to select POR delay times of 12 or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms. When the PORSEL pin is connected to V_{CC}, the POR time is 12 ms.

产品种类:	FPGA - 现场可编程门阵列	☑
RoHS:	N	
产品:	Stratix II	☐
系列:	Stratix II EP2S15	☐
逻辑元件数量:	15600 LE	☐
自适应逻辑模块 - ALM:	6240 ALM	☐
嵌入式内存:	409.5 kbit	☐
输入/输出端数量:	366 I/O	☐
工作电源电压:	1.2 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 70 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-672	☐
封装:	Tray	☐
商标:	Intel / Altera	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	780 LAB	
工作电源电流:	250 mA	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	40	
子类别:	Programmable Logic ICs	
总内存:	419328 bit	
商标名:	Stratix II	
零件号别名:	966856	

芯片详细信息

Manufacturer Part Number: EP2S15F672C5	Rohs Code: No	Part Life Cycle Code: Not Recommended	Ihs Manufacturer: INTEL CORP
Package Description: 35 X 35 MM, 1 MM PITCH, FBGA-672	Reach Compliance Code: compliant	ECCN Code: 3A991	HTS Code: 8542.39.00.01
Manufacturer: Intel Corporation	Risk Rank: 5.3	Clock Frequency-Max: 640 MHz	Combinatorial Delay of a CLB-Max: 5.962 ns
JESD-30 Code: S-PBGA-B672	JESD-609 Code: e0	Length: 35 mm	Moisture Sensitivity Level: 3
Number of CLBs: 6240	Number of Inputs: 366	Number of Logic Cells: 15600	Number of Outputs: 358
Number of Terminals: 672	Operating Temperature-Max: 85 °C	Organization: 6240 CLBS	Package Body Material: PLASTIC/EPOXY
Package Code: BGA	Package Equivalence Code: BGA672,26X26,40	Package Shape: SQUARE	Package Style: GRID ARRAY
Peak Reflow Temperature (Cel): 220	Power Supplies: 1.2,1.5/3.3,3.3 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified
Seated Height-Max: 2.6 mm	Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V
Supply Voltage-Nom: 1.2 V	Surface Mount: YES	Technology: CMOS	Temperature Grade: OTHER
Terminal Finish: TIN LEAD	Terminal Form: BALL	Terminal Pitch: 1.27 mm	Terminal Position: BOTTOM
Time@Peak Reflow Temperature-Max (s): 30	Width: 35 mm		