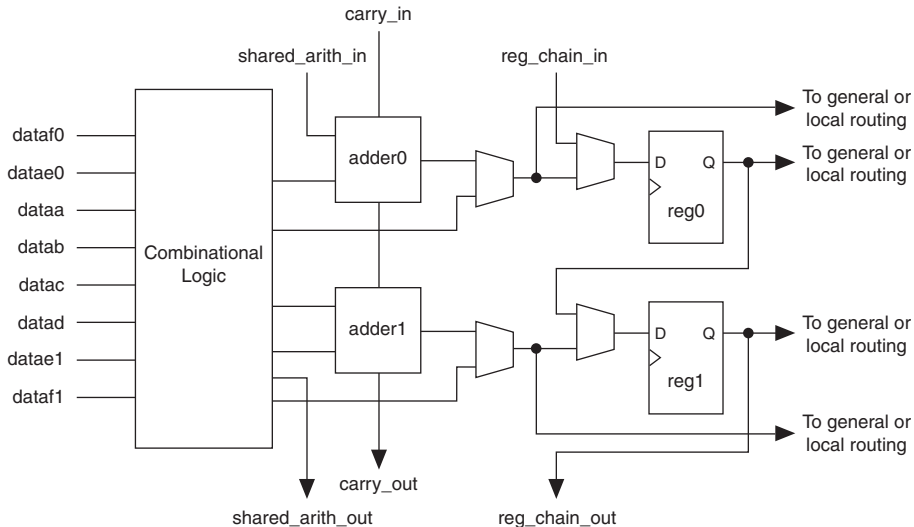


## Adaptive Logic Modules


The basic building block of logic in the Stratix II GX architecture is the ALM. The ALM provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–35 shows a high-level block diagram of the Stratix II GX ALM while Figure 2–36 shows a detailed view of all the connections in the ALM.

**Figure 2–35. High-Level Block Diagram of the Stratix II GX ALM**



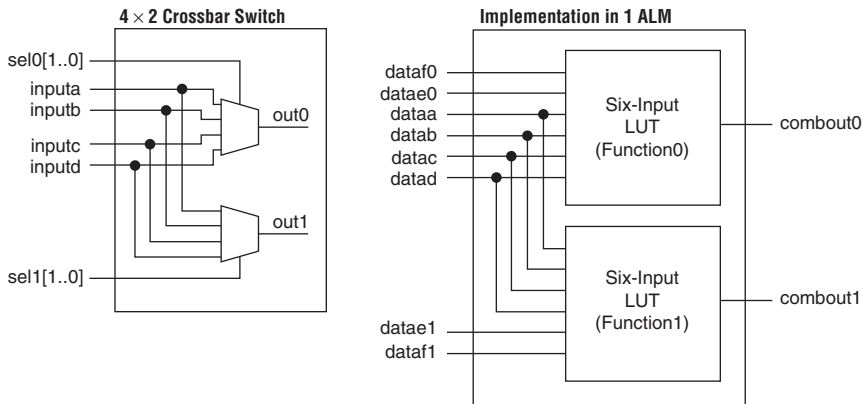
## 芯片详细信息

Manufacturer Part Number: EP2S15F672C4	Rohs Code:  No	Part Life Cycle Code: Not Recommended	Ihs Manufacturer: INTEL CORP
Package Description: 35 X 35 MM, 1 MM PITCH, FBGA-672	Reach Compliance Code: compliant	ECCN Code: 3A991	HTS Code: 8542.39.00.01
Manufacturer: Intel Corporation	Risk Rank: 5,26	Clock Frequency-Max: 717 MHz	Combinatorial Delay of a CLB-Max: 5.117 ns
JESD-30 Code: S-PBGA-B672	JESD-609 Code: e0	Length: 35 mm	Moisture Sensitivity Level: 3
Number of CLBs: 6240	Number of Inputs: 366	Number of Logic Cells: 15600	Number of Outputs: 358
Number of Terminals: 672	Operating Temperature-Max: 85 °C	Organization: 6240 CLBS	Package Body Material: PLASTIC/EPOXY
Package Code: BGA	Package Equivalence Code: BGA672,26X26,40	Package Shape: SQUARE	Package Style: GRID ARRAY
Peak Reflow Temperature (Cel): 220	Power Supplies: 1.2,1.5/3.3,3.3 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified
Seated Height-Max: 2.6 mm	Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.25 V	Supply Voltage-Min: 1.15 V
Supply Voltage-Nom: 1.2 V	Surface Mount: YES	Technology: CMOS	Temperature Grade: OTHER
Terminal Finish: TIN LEAD	Terminal Form: BALL	Terminal Pitch: 1.27 mm	Terminal Position: BOTTOM
Time@Peak Reflow Temperature- Max (s): 30	Width: 35 mm		

To pack two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are `dataaa` and `datab`. The combination of a four-input function with a five-input function requires one common input (either `dataaa` or `datab`).

To implement two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a  $4 \times 2$  crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in [Figure 2–38](#). The shared inputs are `dataaa`, `datab`, `dataac`, and `datad`, while the unique select lines are `datae0` and `dataf0` for `function0`, and `datae1` and `dataf1` for `function1`. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

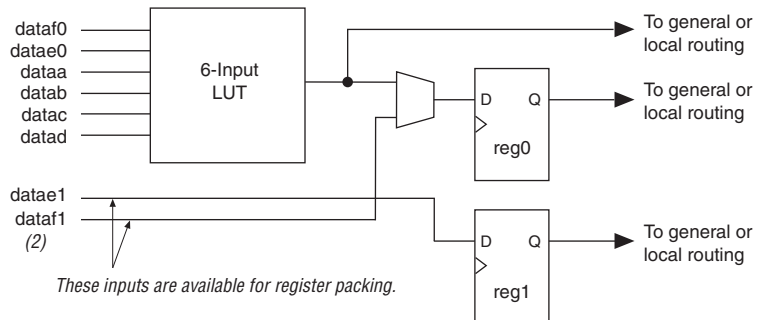
**Figure 2–38.  $4 \times 2$  Crossbar Switch Example**



In a sparsely used device, functions that could be placed into one ALM can be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically utilizes the full potential of the Stratix II GX ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments. Any six-input function can be implemented utilizing inputs `dataaa`, `datab`, `dataac`, `datad`, and either `datae0` and `dataf0` or `datae1` and `dataf1`. If `datae0` and `dataf0` are utilized, the output is driven to `register0`, and/or `register0` is bypassed and the data drives out to the interconnect using the top set of output drivers (see [Figure 2–39](#)). If `datae1` and `dataf1` are utilized, the output drives to `register1` and/or bypasses `register1` and drives to the interconnect

using the bottom set of output drivers. The Quartus II Compiler automatically selects the inputs to the LUT. Asynchronous load data for the register comes from the `dataae` or `dataaf` input of the ALM. ALMs in normal mode support register packing.

**Figure 2–39. 6-Input Function in Normal Mode** Notes (1), (2)



**Notes to Figure 2–39:**

- (1) If `datae1` and `dataf1` are used as inputs to the six-input function, `datae0` and `dataf0` are available for register packing.
- (2) The `dataf1` input is available for register packing only if the six-input function is un-registered.

### Extended LUT Mode

The extended LUT mode is used to implement a specific set of seven-input functions. The set must be a 2-to-1 multiplexer fed by two arbitrary five-input functions sharing four inputs. Figure 2–40 shows the template of supported seven-input functions utilizing extended LUT mode. In this mode, if the seven-input function is unregistered, the unused eighth input is available for register packing. Functions that fit into the template shown in Figure 2–40 occur naturally in designs. These functions often appear in designs as “if-else” statements in Verilog HDL or VHDL code.

产品种类:	FPGA - 现场可编程门阵列	<input checked="" type="checkbox"/>
RoHS:	N	
产品:	Stratix II	<input type="checkbox"/>
系列:	Stratix II EP2S15	<input type="checkbox"/>
逻辑元件数量:	15600 LE	<input type="checkbox"/>
自适应逻辑模块 - ALM:	6240 ALM	<input type="checkbox"/>
嵌入式内存:	409.5 kbit	<input type="checkbox"/>
输入/输出端数量:	366 I/O	<input type="checkbox"/>
工作电源电压:	1.2 V	<input type="checkbox"/>
最小工作温度:	0 C	<input type="checkbox"/>
最大工作温度:	+ 70 C	<input type="checkbox"/>
安装风格:	SMD/SMT	<input type="checkbox"/>
封装 / 箱体:	FBGA-672	<input type="checkbox"/>
封装:	Tray	<input type="checkbox"/>
商标:	Intel / Altera	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	780 LAB	
工作电源电流:	250 mA	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	40	
子类别:	Programmable Logic ICs	
总内存:	419328 bit	
商标名:	Stratix II	
零件号别名:	972226	