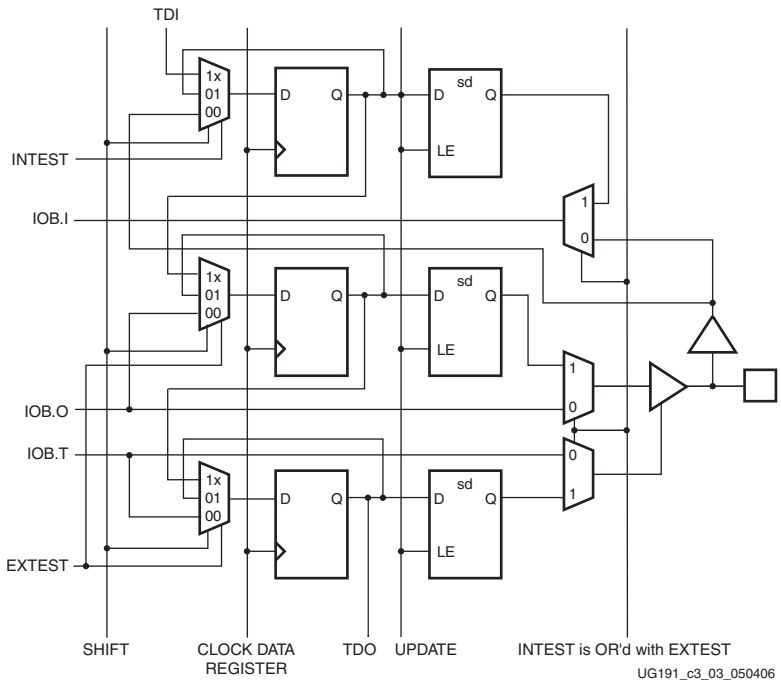


*Figure 3-3:* **Virtex-5 Family Boundary-Scan Logic**

### Bit Sequence Boundary-Scan Register

The order of each non-TAP IOB is described in this section. The input is first, then the output, and finally the 3-state IOB control. The 3-state IOB control is closest to the TDO. The input-only pins contribute only the input bit to the Boundary-Scan I/O data register. The bit sequence of the device is obtainable from the *Boundary-Scan Description Language Files* (BSDL files) for the Virtex-5 family. (These files can be obtained from the Xilinx software download area.) The bit sequence always has the same bit order and the same number of bits and is independent of the design.

## Instruction Register

The Instruction Register (IR) for the Virtex-5 device is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel-loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI.

To determine the operation to be invoked, an OPCODE necessary for the Virtex-5 Boundary-Scan instruction set is loaded into the Instruction Register. The length of the IR is device size-specific. The IR is 10 bits wide for the Virtex-5 LX, LXT, SXT, FXT, and TXT platform devices. The FX100T, FX130T, and FX200T have 14 bits of OPCODE because they contain 2 PowerPC processors. The 4 or 8 most significant bits support the PowerPC 440 embedded processor. The least significant 6 bits of the instruction code perform the same function for all Virtex-5 family members to support the new IEEE Standard 1532 for ISC devices. For PPC JTAG instruction, the least bits must be set to `100000` (20h). For PPC440 JTAG guidelines, refer to UG200, *Embedded Processor Block in Virtex-5 FPGAs Reference Guide*. Table 3-3 lists the available instructions for Virtex-5 devices.

| | | |
|---|---|---|
| 产品种类: | FPGA - 现场可编程门阵列 | ☑ |
| 产品: | Virtex-II Pro | ☐ |
| 系列: | XC2VP20 | ☐ |
| 逻辑元件数量: | 20880 LE | ☐ |
| 自适应逻辑模块 - ALM: | 9280 ALM | ☐ |
| 嵌入式内存: | 1.55 Mbit | ☐ |
| 输入/输出端数量: | 404 I/O | ☐ |
| 工作电源电压: | 1.5 V | ☐ |
| 最小工作温度: | - 40 C | ☐ |
| 最大工作温度: | + 100 C | ☐ |
| 安装风格: | SMD/SMT | ☐ |
| 封装 / 箱体: | FBGA-676 | ☐ |
| 数据速率: | 6.25 Gb/s | |
| 商标: | Xilinx | |
| 分布式RAM: | 290 kbit | |
| 内嵌式块RAM - EBR: | 1584 kbit | |
| 最大工作频率: | 350 MHz | |
| 湿度敏感性: | Yes | |
| 逻辑数组块数量——LAB: | 2320 LAB | |
| 收发器数量: | 8 Transceiver | |
| 产品类型: | FPGA - Field Programmable Gate Array | |
| 工厂包装数量: | 1 | |
| 子类别: | Programmable Logic ICs | |
| 商标名: | Virtex | |

芯片详细信息

| | | | |
|---|---|---|---|
| Manufacturer Part Number:<br>XC2VP20-6FG676I | Pbfree Code:<br>No | Rohs Code:<br>No | Part Life Cycle Code:<br>Obsolete |
| Ihs Manufacturer:<br>XILINX INC | Part Package Code:<br>BGA | Package Description:<br>BGA, BGA676,26X26,40 | Pin Count:<br>676 |
| Reach Compliance Code:<br>not_compliant | ECCN Code:<br>3A991.D | HTS Code:<br>8542.39.00.01 | Factory Lead Time:<br>12 Weeks |
| Manufacturer:<br>Xilinx | Risk Rank:<br>8.73 | Clock Frequency-Max:<br>1200 MHz | Combinatorial Delay of a CLB-Max:<br>0.32 ns |
| JESD-30 Code:<br>S-PBGA-B676 | JESD-609 Code:<br>e0 | Length:<br>27 mm | Moisture Sensitivity Level:<br>3 |
| Number of CLBs:<br>2320 | Number of Inputs:<br>404 | Number of Logic Cells:<br>20880 | Number of Outputs:<br>404 |
| Number of Terminals:<br>676 | Operating Temperature-Max:<br>100 °C | Operating Temperature-Min:<br>-40 °C | Organization:<br>2320 CLBS |
| Package Body Material:<br>PLASTIC/EPOXY | Package Code:<br>BGA | Package Equivalence Code:<br>BGA676,26X26,40 | Package Shape:<br>SQUARE |
| Package Style:<br>GRID ARRAY | Peak Reflow Temperature (Cel):<br>225 | Programmable Logic Type:<br>FIELD PROGRAMMABLE GATE ARRAY | Qualification Status:<br>Not Qualified |
| Seated Height-Max:<br>2.44 mm | Subcategory:<br>Field Programmable Gate Arrays | Supply Voltage-Max:<br>1.575 V | Supply Voltage-Min:<br>1.425 V |
| Supply Voltage-Nom:<br>1.5 V | Surface Mount:<br>YES | Technology:<br>CMOS | Temperature Grade:<br>INDUSTRIAL |
| Terminal Finish:<br>Tin/Lead (Sn63Pb37) | Terminal Form:<br>BALL | Terminal Pitch:<br>1 mm | Terminal Position:<br>BOTTOM |
| Time@Peak Reflow Temperature-Max (s):<br>30 | Width:<br>27 mm | | |

*Table 6-10:* **Configuration Options Register 0 Description *(Continued)***

| Name | Bit Index | Description |
|---|---|---|
| MATCH_CYCLE | [11:9] | Startup cycle to stall in until DCI matches.<br>000: Startup phase 0<br>001: Startup phase 1<br>010: Startup phase 2<br>011: Startup phase 3<br>100: Startup phase 4<br>101: Startup phase 5<br>110: Startup phase 6<br>111: No Wait |
| LOCK_CYCLE | [8:6] | Startup cycle to stall in until DCMs lock.<br>000: Startup phase 0<br>001: Startup phase 1<br>010: Startup phase 2<br>011: Startup phase 3<br>100: Startup phase 4<br>101: Startup phase 5<br>110: Startup phase 6<br>111: No Wait |
| GTS_CYCLE | [5:3] | Startup cycle to deassert the Global Three-State (GTS) signal.<br>000: Startup phase 1<br>001: Startup phase 2<br>010: Startup phase 3<br>011: Startup phase 4<br>100: Startup phase 5<br>101: Startup phase 6<br>110: GTS tracks DONE pin. BitGen option **-g GTS_cycle:Done**<br>001: Keep |
| GWE_CYCLE | [2:0] | Startup phase to deassert the Global Write Enable (GWE) signal.<br>000: Startup phase 1<br>001: Startup phase 2<br>010: Startup phase 3<br>011: Startup phase 4<br>100: Startup phase 5<br>101: Startup phase 6<br>110: GWE tracks DONE pin. BitGen option **-g GWE_cycle:Done**<br>111: Keep |

## Configuration Options Register 1 (COR1)

The Configuration Options Register 1 is used to set certain configuration options for the device. The name of each bit position in the COR1 is given in Figure 6-5 and described in Table 6-11.

| Description | Reserved | PERSIST_DEASSERT_AT_DESYNCH | Reserved | Reserved | RBCRC_NO_PIN | RBCRC_EN | Reserved | BPI_1ST_READ_CYCLES | BPI_PAGE_SIZE |
|---|---|---|---|---|---|---|---|---|---|
| Bit Index | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 | 17 | 16 | 15 14 13 12 11 10 | 9 | 8 | 7 6 5 4 | 3 2 | 1 0 |
| Value | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | 0 | 0 | 0 0 0 0 0 0 | 0 | 0 | 0 0 0 0 | 0 0 | 0 0 |

*Figure 6-5:* **Configuration Options Register 1**

*Table 6-11:* **Configuration Options Register 1 Description**

| Name | Bit Index | Description |
|---|---|---|
| PERSIST_DEASSERT_AT_DESYNCH | 17 | Enables deassertion of PERSIST with the DESYNCH command |
| RBCRC_NO_PIN | 9 | Disables INIT_B as read back CRC error status output pin |
| RBCRC_EN | 8 | Continuous readback CRC enable |
| BPI_1ST_READ_CYCLES | [3:2] | First byte read timing:<br>00: 1 CCLK<br>01: 2 CCLKs<br>10: 3 CCLKs<br>11: 4 CCLKs |
| BPI_PAGE_SIZE | [1:0] | Flash memory page size:<br>00: 1 byte/word<br>01: 4 bytes/words<br>10: 8 bytes/words<br>11: Reserved |

## Warm Boot Start Address Register (WBSTAR)

The name of each bit position in the WBSTAR is given in Figure 6-6 and described in Table 6-12.