Chapter 6

GTX Transmitter (TX)

This chapter shows how to configure and use each of the functional blocks inside the GTX transmitter.

Transmitter Overview

Each GTX transceiver in the GTX_DUAL tile includes an independent transmitter, which consists of a PCS and a PMA. Figure 6-1 shows the functional blocks of the transmitter. Parallel data flows from the FPGA into the FPGA TX interface, through the PCS and PMA, and then out the TX driver as high-speed serial data. Refer to Appendix E, "Low Latency Design," for latency information on this block diagram.

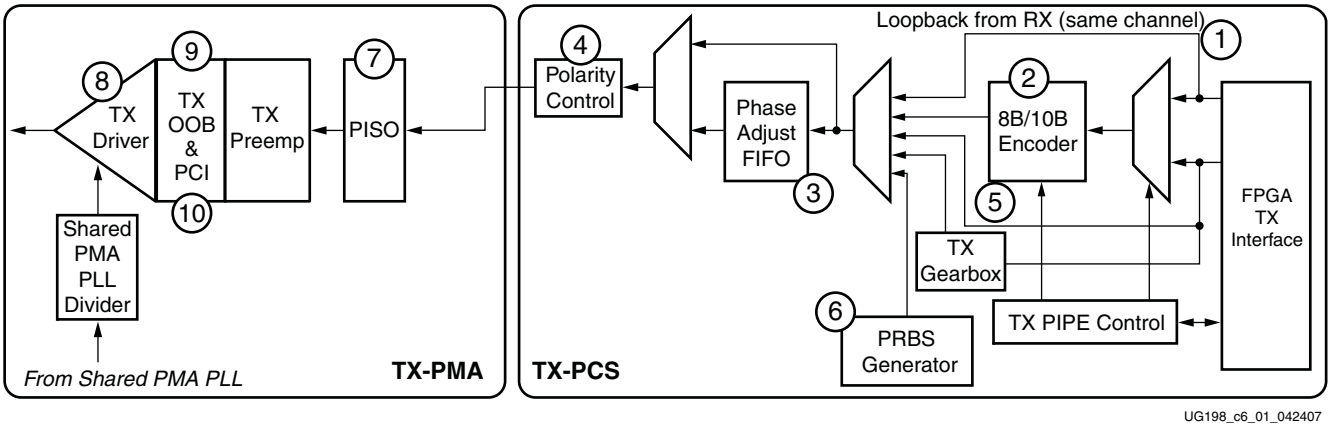

Figure 6-1: **GTX TX Block Diagram**

The key elements within the GTX transmitter are:

1. "FPGA TX Interface," page 120
2. "Configurable 8B/10B Encoder," page 129
3. "TX Buffering, Phase Alignment, and TX Skew Reduction," page 141
4. "TX Polarity Control," page 147
5. "TX Gearbox," page 134
6. "TX PRBS Generator," page 148
7. "Parallel In to Serial Out," page 149
8. "Configurable TX Driver," page 150
9. "Receive Detect Support for PCI Express Operation," page 153
10. "TX Out-of-Band/Beacon Signaling," page 157

Description

Enabling 8B/10B Encoding

To disable the 8B/10B encoder on a given GTX transceiver, TXENC8B10BUSE must be driven Low. To enable the 8B/10B encoder, TXENC8B10BUSE must be driven High. When the encoder is turned off, the operation of the TXDATA port is as described in "FPGA TX Interface."

8B/10B Bit and Byte Ordering

The order of the bits after the 8B/10B encoder is the opposite of the order shown in Appendix C, "8B/10B Valid Characters," because 8B/10B encoding requires bit a0 to be transmitted first, and the GTX transceiver always transmits the right-most bit first. To match with 8B/10B, the 8B/10B encoder in the GTX transceiver automatically reverses the bit order (Figure 6-10).

For the same reason, when a 2-byte interface is used, the first byte to be transmitted (byte 0) must be placed on TXDATA[7:0], and the second placed on TXDATA[15:8]. When a 4-byte interface is used, byte 0 must be placed on TXDATA[7:0], byte 1 must be placed on TXDATA[15:8], byte 2 must be placed on TXDATA[23:16], and byte 3 must be placed on TXDATA[31:24]. This placement ensures that the byte 0 bits are all sent before the byte 1 bits, as required by 8B/10B encoding.

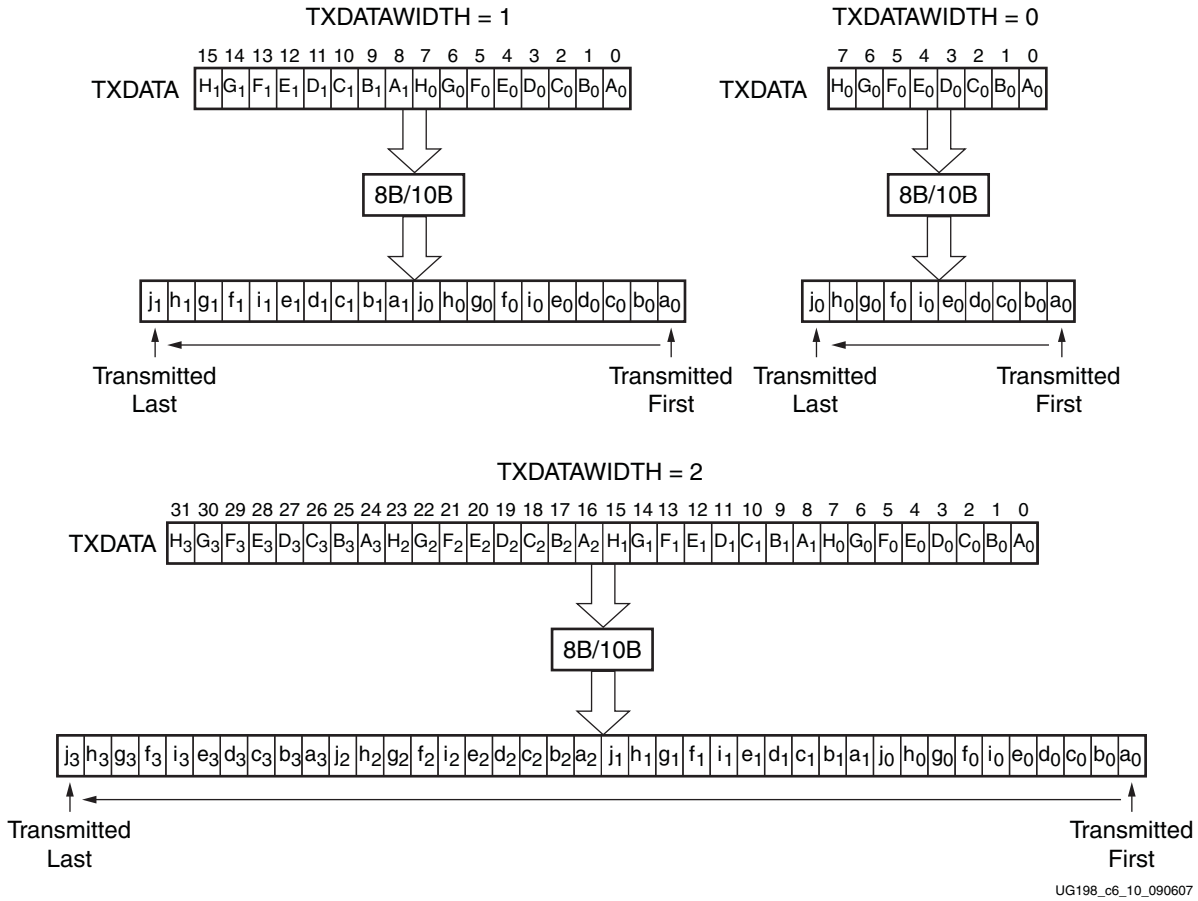

Figure 6-10: **8B/10B Encoding**

or TXRESET (see "FPGA TX Interface," page 120). Assertion of GTXRESET triggers a sequence that resets the entire GTX_DUAL tile.

Using the TX Phase-Alignment Circuit to Minimize TX Skew

To use the phase-alignment circuit to force the XCLK phase of multiple lanes to match the common TXUSRCLK phase, follow these steps.

Initial conditions when TX_BUFFER_USE is TRUE:

- Set TX_BUFFER_USE_0 and TX_BUFFER_USE_1 to TRUE.
- Set TXRX_INVERT0 and TXRX_INVERT1 to 011.
- Set TX_XCLK_SEL0 and TX_XCLK_SEL1 to TXOUT.
- Set PMA_TX_CFG0 and PMA_TX_CFG1 to `20'h80082`.

1. Set TX_XCLK_SEL0 and TX_XCLK_SEL1 to *TXUSR*.
2. Wait for all clocks to stabilize, then drive TXENPMAPHASEALIGN High.

   Keep TXENPMAPHASEALIGN High unless the phase-alignment procedure must be repeated. Driving TXENPMAPHASEALIGN Low causes phase alignment to be lost.
3. Wait 32 TXUSRCLK2 clock cycles, and then drive TXPMASETPHASE High.
4. Wait the number of required TXUSRCLK2 clock cycles as specified in Table 6-11, and then drive TXPMASETPHASE Low. The phase of the PMACLK is now aligned with TXUSRCLK.
5. Set TX_XCLK_SEL0 and TX_XCLK_SEL1 back to *TXOUT.*
6. Assert and deassert TXRESET synchronously to TXUSRCLK. In this use mode, TXRESET must be deasserted simultaneously to all GTX Transceivers on which the deskew operation is being performed.

Table 6-11: **Number of Required TXUSRCLK2 Clock Cycles**

PLL_DIVSEL_OUT_0 PLL_DIVSEL_OUT_1	TXUSRCLK2 Wait Cycles
1	8,192
2	16,384
4	32,767

The phase-alignment procedure must be redone if any of the following conditions occur:

- GTXRESET is asserted
- PLLPOWERDOWN is deasserted
- The clocking source changed

Figure 6-20 shows the TX phase-alignment procedure. TXENPMAPHASEALIGN(0/1) and TXPMASETPHASE(0/1) are independent for each GTX transceiver. This implementation is different from the GTP_DUAL tile where TXENPHASEALIGN and TXPMASETPHASE are shared tile pins. The procedure is always applied to each GTX transceiver's TXENPMAPHASEALIGN(0/1) signal on the tile. TXOUTCLK cannot be the source for TXUSRCLK when the TX phase-alignment circuit is used. See "FPGA TX Interface," page 120 for details.

芯片详细信息

Manufacturer Part Number: XC2VP20-6FG676C	Pbfree Code: No	Rohs Code: No	Part Life Cycle Code: Obsolete
Ihs Manufacturer: XILINX INC	Part Package Code: BGA	Package Description: BGA, BGA676,26X26,40	Pin Count: 676
Reach Compliance Code: not_compliant	ECCN Code: 3A991.D	HTS Code: 8542.39.00.01	Factory Lead Time: 12 Weeks
Manufacturer: Xilinx	Risk Rank: 5.83	Clock Frequency-Max: 1200 MHz	Combinatorial Delay of a CLB-Max: 0.32 ns
JESD-30 Code: S-PBGA-B676	JESD-609 Code: e0	Length: 27 mm	Moisture Sensitivity Level: 3
Number of CLBs: 2320	Number of Inputs: 404	Number of Logic Cells: 20880	Number of Outputs: 404
Number of Terminals: 676	Operating Temperature-Max: 85 °C	Organization: 2320 CLBS	Package Body Material: PLASTIC/EPOXY
Package Code: BGA	Package Equivalence Code: BGA676,26X26,40	Package Shape: SQUARE	Package Style: GRID ARRAY
Peak Reflow Temperature (Cel): 225	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 2.44 mm
Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.575 V	Supply Voltage-Min: 1.425 V	Supply Voltage-Nom: 1.5 V
Surface Mount: YES	Technology: CMOS	Temperature Grade: OTHER	Terminal Finish: Tin/Lead (Sn63Pb37)
Terminal Form: BALL	Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 30
Width: 27 mm			

产品种类:	FPGA - 现场可编程门阵列	☑
产品:	Virtex-II Pro	☐
系列:	XC2VP20	☐
逻辑元件数量:	20880 LE	☐
自适应逻辑模块 - ALM:	9280 ALM	☐
嵌入式内存:	1.55 Mbit	☐
输入/输出端数量:	404 I/O	☐
工作电源电压:	1.5 V	☐
最小工作温度:	0 C	☐
最大工作温度:	+ 85 C	☐
安装风格:	SMD/SMT	☐
封装 / 箱体:	FBGA-676	☐
数据速率:	6.25 Gb/s	
商标:	Xilinx	
分布式RAM:	290 kbit	
内嵌式块RAM - EBR:	1584 kbit	
最大工作频率:	350 MHz	
湿度敏感性:	Yes	
逻辑数组块数量——LAB:	2320 LAB	
收发器数量:	8 Transceiver	
产品类型:	FPGA - Field Programmable Gate Array	
工厂包装数量:	1	
子类别:	Programmable Logic ICs	
商标名:	Virtex	