Configuration Registers

Table 5-30 summarizes the configuration registers. A detailed explanation of selected registers follows.

Table 5-30: **Configuration Registers**

Register Name	R/W	Address	Description
CRC	W	6'h00	Cyclic Redundancy Check.
FAR_MAJ	W	6'h01	Frame Address Register Block and Major.
FAR_MIN	W	6'h02	Frame Address Register Minor.
FDRI	W	6'h03	Frame Data Input.
FDRO	R	6'h04	Frame Data Output.
CMD	R/W	6'h05	Command.
CTL	R/W	6'h06	Control.
MASK	R/W	6'h07	Control Mask.
STAT	R	6'h08	Status.
LOUT	W	6'h09	Legacy output for serial daisy-chain.
COR1	R/W	6'h0a	Configuration Option 1.
COR2	R/W	6'h0b	Configuration Option 2.
PWRDN_REG	R/W	6'h0c	Power-down Option register.
FLR	W	6'h0d	Frame Length register.
IDCODE	R/W	6'h0e	Product IDCODE.
CWDT	R/W	6'h0f	Configuration Watchdog Timer.
HC_OPT_REG	R/W	6'h10	House Clean Option register.
CSBO	W	6'h12	CSB output for parallel daisy-chaining.
GENERAL1	R/W	6'h13	Power-up self test or loadable program address.
GENERAL2	R/W	6'h14	Power-up self test or loadable program address and new SPI opcode.
GENERAL3	R/W	6'h15	Golden bitstream address.
GENERAL4	R/W	6'h16	Golden bitstream address and new SPI opcode.
GENERAL5	R/W	6'h17	User-defined register for fail-safe scheme.
MODE_REG	R/W	6'h18	Reboot mode.
PU_GWE	W	6'h19	GWE cycle during wake-up from suspend.
PU_GTS	W	6'h1a	GTS cycle during wake-up from suspend.
MFWR	W	6'h1b	Multi-frame write register.
CCLK_FREQ	W	6'h1c	CCLK frequency select for master mode.

Table 5-30: **Configuration Registers *(Cont'd)***

Register Name	R/W	Address	Description
SEU_OPT	R/W	6'h1d	SEU frequency, enable and status.
EXP_SIGN	R/W	6'h1e	Expected readback signature for SEU detection.
RDBK_SIGN	W	6'h1f	Readback signature for readback command and SEU.
BOOTSTS	R	6'h20	Boot History Register.
EYE_MASK	R/W	6'h21	Mask pins for Multi-Pin Wake-Up.
CBC_REG	W	6'h22	Initial CBC Value Register.

CRC Register

The Cyclic Redundancy Check register utilizes a standard 32-bit CRC checksum algorithm to verify bitstream integrity during configuration. If the value written matches the current calculated CRC, the CRC_ERROR flag is cleared and startup is allowed.

FAR_MAJ Register

Frame Address Register sets the starting block and column address for the next configuration data input. See Table 5-31.

Table 5-31: **Frame Address Register (MAJOR)**

	BLK	ROW	MAJOR
Bits	[15:12]	[11:8]	[7:0]
	0xxx	xxxx	xxxxxxxx

FAR_MIN Register

Table 5-32: **Frame Address Register (MINOR)**

	Block RAM	(Reserved)	MINOR
Bits	[15:14]	[13:10]	[9:0]
	xx	0000	xxxxxxxxxx

There are three types of write to FAR:

- Write one word to FAR_MAJ: only updates the FAR_MAJ.
- Write one word to FAR_MIN: only updates the FAR_MIN.
- Write two words to FAR_MAJ: updates both FAR_MAJ and FAR_MIN; the data for FAR_MAJ will come first.

FDRI Register

Configuration data is written to the device by loading the command register with the WCFG command and then loading the Frame Data Input Register.

芯片详细信息

Manufacturer Part Number: XC2VP20-6FFG1152I	Pbfree Code: Yes	Rohs Code: Yes	Part Life Cycle Code: Obsolete
Ihs Manufacturer: XILINX INC	Part Package Code: BGA	Package Description: BGA, BGA1152,34X34,40	Pin Count: 1152
Reach Compliance Code: not_compliant	ECCN Code: 3A991.D	HTS Code: 8542.39.00.01	Manufacturer: Xilinx
Risk Rank: 5.79	Clock Frequency-Max: 1200 MHz	Combinatorial Delay of a CLB-Max: 0.32 ns	JESD-30 Code: S-PBGA-B1152
JESD-609 Code: e1	Length: 35 mm	Moisture Sensitivity Level: 4	Number of CLBs: 2320
Number of Inputs: 564	Number of Logic Cells: 20880	Number of Outputs: 564	Number of Terminals: 1152
Organization: 2320 CLBS	Package Body Material: PLASTIC/EPOXY	Package Code: BGA	Package Equivalence Code: BGA1152,34X34,40
Package Shape: SQUARE	Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 245	Power Supplies: 1.5,1.5/3.3,2/2.5,2.5 V
Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 3.4 mm	Subcategory: Field Programmable Gate Arrays
Supply Voltage-Max: 1.575 V	Supply Voltage-Min: 1.425 V	Supply Voltage-Nom: 1.5 V	Surface Mount: YES
Technology: CMOS	Terminal Finish: Tin/Silver/Copper (Sn95.5Ag4.0Cu0.5)	Terminal Form: BALL	Terminal Pitch: 1 mm
Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 30	Width: 35 mm	

XC3S1400A-4FTG256C	2001+	BGA256	2315
XC3S1400A-4FT256I	2001+	BGA	2315
XC3S1400A-4FT256C	2001+	BGA	2315
XC3S1400A-4FGG676I	2001+	BGA676	2315
XC3S1400A-4FGG676I	2001+	BGA676	2315
XC3S1400A-4FGG676C	2001+	BGA676	2315
XC3S1400A-4FGG676C	2001+	BGA676	2315
XC3S1400A-4FGG676	2001+	BGA	2315
XC3S1400A-4FGG485I	2001+	BGA	2315
XC3S1400A-4FGG484I	2001+	BGA484	2315
XC3S1400A-4FGG484I	2001+	BGA484	2315
XC3S1400A-4FGG484C	2001+	BGA484	2315
XC3S1400A-4FGG484C	2001+	BGA484	2315
XC3S1400A-4FGG484C	2001+	BGA484	2315
XC3S1400A-4FGG484	2001+	BGA	2315
XC3S1400A-4FGG484	2001+	BGA	2315
XC3S1400A-4FG676I	2001+	BGA	2315
XC3S1400A-4FG676C	2001+	BGA	2315
XC3S1400A-4FG676	2001+	BGA	2315
XC3S1400A4FG676	2001+	BGA	2315
XC3S1400A-4FG484I	2001+	BGA484	2315
XC3S1400A-4FG484C	2001+	BGA	2315
XC3S1400A-4FG484	2001+	BGA	2315
XC3S1400A-4	2001+	BGA	2315
XC3S1400A-10FTG256C	2001+	BGA	2315
XC3S1400A/AN	2001+	BGA	2315
XC3S1400A	2001+	BGA	2315
XC3S1400 4FG676C	2001+	FCBGA	2315
XC3S12E4FGG320I	2001+	BGA	2315
XC3S1200E-FTG256C	2001+	BGA	2315
XC3S1200E-FTG256	2001+	BGA	2315
XC3S1200EFTG256	2001+	BGA	2315
XC3S1200E-FT256AGQ	2001+	BGA	2315
XC3S1200E-FT256	2001+	BGA	2315
XC3S1200E-FGG400DGQ	2001+	BGA	2315
XC3S1200E-FGG400	2001+	BGA	2315
XC3S1200EFGG400	2001+	BGA	2315
XC3S1200E-FGG320AGQ	2001+	BGA	2315
XC3S1200EFGG320-4C	2001+	BGA	2315
XC3S1200EFGG320	2001+	BGA	2315
XC3S1200E-FG400	2001+	BGA	2315

2. The INIT_B pin is a bidirectional, open-drain pin. An external pull-up resistor is required.
3. The BitGen startup clock setting must be set for CCLK for serial configuration.
4. The PROM in this diagram represents one or more Xilinx® PROMs. Multiple Xilinx PROMs can be cascaded to increase the overall configuration storage capacity.
5. The **`BIT`** file must be reformatted into a PROM file before it can be stored on the Xilinx PROM.
6. The CCLK net requires Thevenin parallel termination. See Board Layout for Configuration Clock (CCLK), page 56.
7. Serial daisy-chains are specific to the Platform Flash (XCFxxS and XCFxxP) PROMs and SPI serial flash only.

The first device in a serial daisy-chain is the last to be configured. CRC checks only include the data for the current device, not for any others in the chain.

After the last device in the chain finishes configuration and passes its CRC check, it enters the Startup sequence. At the *Release DONE pin* phase in the Startup sequence, the device places its DONE pin in a High-Z state while the next to the last device in the chain is configured. After all devices release their DONE pins, the common DONE signal is either pulled High externally or driven High by the first device in the chain. On the next rising CCLK edge, all devices move out of the *Release DONE pin* phase and complete their startup sequences.

It is important that all DONE pins in a Slave Serial daisy-chain be connected. Only the first device in the serial daisy-chain should have the DONE active pull-up driver enabled. Enabling the DONE driver on downstream devices causes contention on the DONE signal.

If using SPI in a serial daisy-chain configuration, the slave FPGAs must be configured with a design prior to attempting to indirectly program the SPI flash through the master FPGA. Not doing so causes indirect programming to fail.

Mixed Serial Daisy-Chains

Spartan-6 devices can be daisy-chained with the Spartan-3, Virtex®-4, and Virtex-5 families. There are three important design considerations when designing a mixed serial daisy-chain:

- Many older FPGA devices cannot accept as fast a CCLK frequency as a Spartan-6 device can generate. Select a configuration CCLK speed supported by all devices in the chain.
- Spartan-6 devices should always be at the beginning of the serial daisy-chain, with older family devices located at the end of the chain.
- These device families have similar BitGen options. The guidelines provided for Spartan-6 FPGA BitGen options should be applied to all devices in a serial daisy-chain.
- The number of configuration bits that a device can pass through its DOUT pin is limited. This limit varies for different families (Table 9-1). The sum of the bitstream lengths for all downstream devices must not exceed the number in Table 9-1 for each family.