Clock Generation

The VC707 board provides five clock sources for the FPGA. Table 1-9 lists the source devices for each clock.

Table 1-9: **VC707 Board Clock Sources**

Clock Name	Clock Source	Description
System Clock	U51	SiT9102 2.5V LVDS 200 MHz Fixed Frequency Oscillator (SiTime). See System Clock (SYSCLK_P and SYSCLK_N).
User Clock	U34	Si570 3.3V LVDS I^2C Programmable Oscillator, 156.250 MHz default (Silicon Labs). See Programmable User Clock (USER_CLOCK_P and USER_CLOCK_N).
User SMA Clock (differential pair)	J31	USER_SMA_CLOCK_P (Net name). See User SMA Clock (USER_SMA_CLOCK_P and USER_SMA_CLOCK_N).
	J32	USER_SMA_CLOCK_N (Net name). See User SMA Clock (USER_SMA_CLOCK_P and USER_SMA_CLOCK_N).
GTX SMA REF Clock (differential pair)	J25	SMA_MGT_REFCLK_C_P (Net name). See GTX SMA Clock (SMA_MGT_REFCLK_P and SMA_MGT_REFCLK_N).
	J26	SMA_MGT_REFCLK_C_N (Net name). See GTX SMA Clock (SMA_MGT_REFCLK_P and SMA_MGT_REFCLK_N).
Jitter Attenuated Clock	U24	Si5324C LVDS precision clock multiplier/jitter attenuator (Silicon Labs). See Jitter Attenuated Clock.

Table 1-10 lists the pin-to-pin connections from each clock source to the FPGA.

Table 1-10: **Clock Connections, Source to FPGA**

Clock Source Pin	Net Name	I/O Standard	FPGA (U1) Pin
U51.5	SYSCLK_N	LVDS	E18
U51.4	SYSCLK_P	LVDS	E19
U34.5	USER_CLOCK_N	LVDS	AL34
U34.4	USER_CLOCK_P	LVDS	AK34
J26.1	SMA_MGT_REFCLK_N	N/A (MGT REFCLK INPUT)	AK7
J25.1	SMA_MGT_REFCLK_P	N/A (MGT REFCLK INPUT)	AK8
J32.1	USER_SMA_CLOCK_N	LVCMOS18	AK32
J31.1	USER_SMA_CLOCK_P	LVCMOS18	AJ32
U24.29	Si5324_OUT_N	N/A (MGT REFCLK INPUT)	AD7
U24.28	Si5324_OUT_P	N/A (MGT REFCLK INPUT)	AD8

System Clock (SYSCLK_P and SYSCLK_N)

[Figure 1-2, callout 7]

The VC707 board has a LVDS 200 MHz oscillator (U51) soldered onto the back side of the board and wired to an FPGA MRCC clock input on bank 38. This 200 MHz signal pair is named SYSCLK_P and SYSCLK_N, which are connected to FPGA U1 pins E19 and E18 respectively.

- Oscillator: SiTime SiT9102AI-243N25E200.00000 (200 MHz)
- PPM frequency tolerance: 50 ppm
- Differential Output

For more details, see the SiTime SiT9102 data sheet [Ref 19]. The system clock circuit is shown in Figure 1-9.

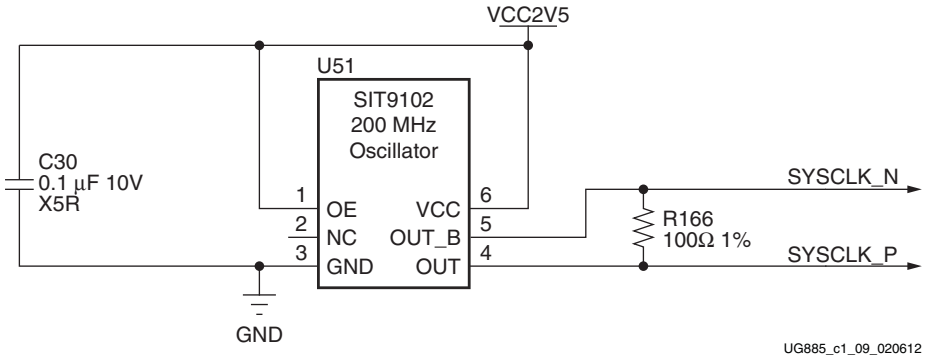

Figure 1-9: **System Clock Source**

Programmable User Clock (USER_CLOCK_P and USER_CLOCK_N)

[Figure 1-2, callout 8]

The VC707 board has a programmable low-jitter 3.3V differential oscillator (U34) connected to the FPGA MRCC inputs of bank 14. This USER_CLOCK_P and USER_CLOCK_N clock signal pair are connected to FPGA U1 pins AK34 and AL34 respectively. On power-up the user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I^2C interface. Power cycling the VC707 board reverts the user clock to its default frequency of 156.250 MHz.

- Programmable Oscillator: Silicon Labs Si570BAB0000544DG (10 MHz - 810 MHz)
- Differential Output

SGMII GTX Transceiver Clock Generation

[Figure 1-2, callout 16]

An Integrated Circuit Systems ICS844021I chip (U2) generates a high-quality, low-jitter, 125 MHz LVDS clock from a 25 MHz crystal (X3). This clock is sent to FPGA U1, Bank 113 GTX transceiver (clock pins AH8 (P) and AH7 (N)) driving the SGMII interface. Series AC coupling capacitors are present to allow the clock input of the FPGA to set the common mode voltage. Figure 1-17 shows the Ethernet SGMII clock source.

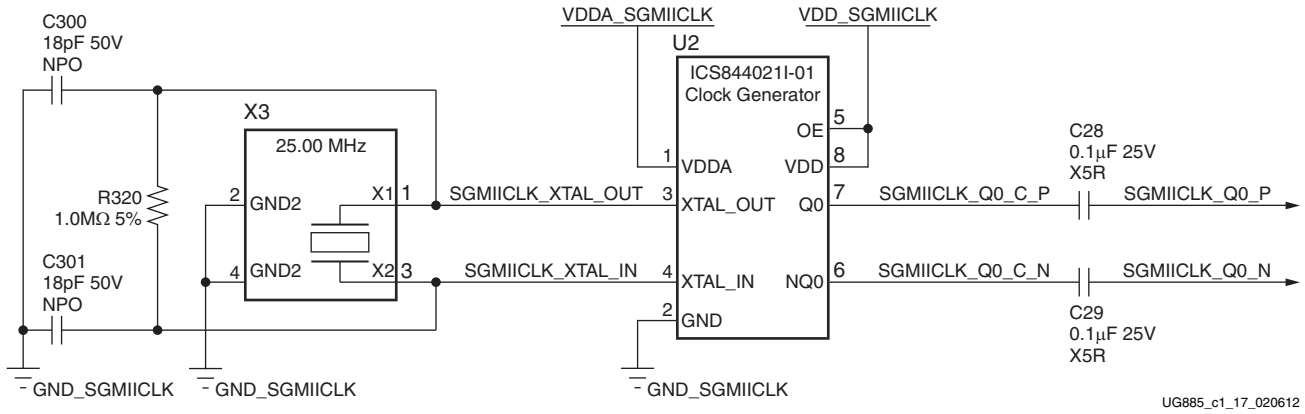

Figure 1-17: **Ethernet 125 MHz SGMII GTX Clock**

References

Details about the tri-mode Ethernet MAC core are provided in *LogiCORE IP Tri-Mode Ethernet MAC Product Guide for Vivado Design Suite* (PG051) [Ref 9] and in the *LogiCORE IP Tri-Mode Ethernet MAC v4.5 User Guide* (UG138) [Ref 13].

The product brief for the Marvell 88E1111 Alaska Gigabit Ethernet Transceiver can be found at the Marvell website [Ref 21].

The data sheet can be obtained under NDA with Marvell. Contact information is at the Marvell website [Ref 21].

For more information about the ICS844021 device, go to the Integrated Device Technology website [Ref 22] and search for part number **ICS844021**.

USB-to-UART Bridge

[Figure 1-2, callout 17]

The VC707 board contains a Silicon Labs CP2103GM USB-to-UART bridge device (U44) which allows a connection to a host computer with a USB port. The USB cable is supplied in the VC707 Evaluation Kit (Type-A end to host computer, Type mini-B end to VC707 board connector J17). The CP2103GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the VC707 board.

Xilinx UART IP is expected to be implemented in the FPGA logic. The FPGA supports the USB-to-UART bridge using four signal pins: Transmit (TX), Receive (RX), Request to Send (RTS), and Clear to Send (CTS).

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers for the host computer. These drivers permit the CP2103GM USB-to-UART bridge to appear as a COM port to communications application software (for example, TeraTerm) that runs on the host computer. The VCP device

芯片详细信息

Manufacturer Part Number: XC2VP20-6FFG896I	Pbfree Code: Yes	Rohs Code: Yes	Part Life Cycle Code: Obsolete
Ihs Manufacturer: XILINX INC	Part Package Code: BGA	Package Description: BGA, BGA896,30X30,40	Pin Count: 896
Reach Compliance Code: not_compliant	ECCN Code: 3A991.D	HTS Code: 8542.39.00.01	Manufacturer: Xilinx
Risk Rank: 5.79	Clock Frequency-Max: 1200 MHz	Combinatorial Delay of a CLB-Max: 0.32 ns	JESD-30 Code: S-PBGA-B896
JESD-609 Code: e1	Length: 31 mm	Moisture Sensitivity Level: 4	Number of CLBs: 2320
Number of Inputs: 556	Number of Logic Cells: 20880	Number of Outputs: 556	Number of Terminals: 896
Organization: 2320 CLBS	Package Body Material: PLASTIC/EPOXY	Package Code: BGA	Package Equivalence Code: BGA896,30X30,40
Package Shape: SQUARE	Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 245	Power Supplies: 1.5,1.5/3.3,2/2.5,2.5 V
Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 3.4 mm	Subcategory: Field Programmable Gate Arrays
Supply Voltage-Max: 1.575 V	Supply Voltage-Min: 1.425 V	Supply Voltage-Nom: 1.5 V	Surface Mount: YES
Technology: CMOS	Terminal Finish: Tin/Silver/Copper (Sn95.5Ag4.0Cu0.5)	Terminal Form: BALL	Terminal Pitch: 1 mm
Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 30	Width: 31 mm	

XC3S1400AN FGG676	2001+	BGA	2315
XC3S1400AN 4FG676C	2001+	FCBGA	2315
XC3S1400AN	2001+	BGA	2315
XC3S1400A-FTG256I	2001+	BGA	2315
XC3S1400A-FTG256	2001+	BGA	2315
XC3S1400AFTG256	2001+	BGA	2315
XC3S1400A-FGG676AGQ	2001+	BGA	2315
XC3S1400AFGG676AGQ	2001+	BGA	2315
XC3S1400A-FGG676	2001+	BGA	2315
XC3S1400AFGG676	2001+	BGA	2315
XC3S1400A-FGG484I	2001+	BGA-484	2315
XC3S1400A-FGG484AGQ	2001+	BGA	2315
XC3S1400A-FGG484	2001+	BGA	2315
XC3S1400AFG676	2001+	BGA	2315
XC3S1400AFG484	2001+	BGA	2315
XC3S1400AFG256	2001+	BGA	2315
XC3S1400A-FG	2001+	BGA	2315
XC3S1400A-5FTG256I	2001+	BGA256	2315
XC3S1400A-5FTG256C	2001+	BGA	2315
XC3S1400A-5FT256I	2001+	BGA	2315
XC3S1400A-5FT256C	2001+	BGA	2315
XC3S1400A-5FGG676I	2001+	BGA	2315
XC3S1400A-5FGG676C	2001+	BGA	2315
XC3S1400A-5FGG676	2001+	BGA	2315
XC3S1400A-5FGG484I	2001+	BGA	2315
XC3S1400A5FGG484C/5I	2001+	BGA	2315
XC3S1400A-5FGG484C	2001+	BGA484	2315
XC3S1400A-5FG676I	2001+	BGA	2315
XC3S1400A-5FG676C	2001+	BGA	2315
XC3S1400A-5FG484I/4C	2001+	BGA	2315
XC3S1400A-5FG484I	2001+	BGA	2315
XC3S1400A-5FG484C	2001+	BGA	2315
XC3S1400A-5/4FGG676	2001+	BGA	2315
XC3S1400A-5/4FGG484	2001+	BGA	2315
XC3S1400A-4GTG256C	2001+	QFP	2315
XC3S1400A-4FTG484	2001+	BGA	2315
XC3S1400A-4FTG256I	2001+	BGA256	2315
XC3S1400A-4FTG256I	2001+	BGA256	2315
XC3S1400A-4FTG256C	2001+	BGA256	2315
XC3S1400A-4FTG256C	2001+	BGA256	2315
XC3S1400A-4FT256I	2001+	BGA	2315