Switching Characteristics

All Spartan-3 devices are available in two speed grades: –4 and the higher performance –5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reported delays may still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Production-quality systems must use FPGA designs compiled using a Production status speed file. FPGAs designs using a less mature speed file designation may only be used during system prototyping or preproduction qualification. FPGA designs using Advance or Preliminary status speed files should never be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All specified limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the following applies: Parameter values apply to all Spartan-3 devices. All parameters representing voltages are measured with respect to GND.

Selected timing parameters and their representative values are included below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3 FPGA v1.38 speed files are the original source for many but not all of the values. The v1.38 speed files are available in Xilinx Integrated Software Environment (ISE) software version 8.2i.

The speed grade designations for these files are shown in Table 39. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 39: **Spartan-3 FPGA Speed Grade Designations (ISE v8.2i or Later)**

Device	Advance	Preliminary	Production
XC3S50			-4, -5 (v1.37 and later)
XC3S200			
XC3S400			
XC3S1000			
XC3S1500			
XC3S2000			
XC3S4000			
XC3S5000			-4, -5 (v1.38 and later)

Table 48: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
HSTL_III_DCI_18							
LVCMOS12		-	0	1.2	1M	0	0.6
LVCMOS15		-	0	1.5	1M	0	0.75
LVDCI_15							
LVDCI_DV2_15							
HSLVDCI_15							
LVCMOS18		-	0	1.8	1M	0	0.9
LVDCI_18							
LVDCI_DV2_18							
HSLVDCI_18							
LVCMOS25		-	0	2.5	1M	0	1.25
LVDCI_25							
LVDCI_DV2_25							
HSLVDCI_25							
LVCMOS33		-	0	3.3	1M	0	1.65
LVDCI_33							
LVDCI_DV2_33							
HSLVDCI_33							
LVTTL		-	0	3.3	1M	0	1.4
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_I_DCI							
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_I_DCI							
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL2_II_DCI					50	1.25	
Differential							
LDT_25 (ULVDS_25)		-	V_{ICM} – 0.125	V_{ICM} + 0.125	60	0.6	V_{ICM}
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_25_DCI					N/A	N/A	
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
LVDSEXT_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDSEXT_25_DCI					N/A	N/A	
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
DIFF_HSTL_II_18		-	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_HSTL_II_18_DCI							

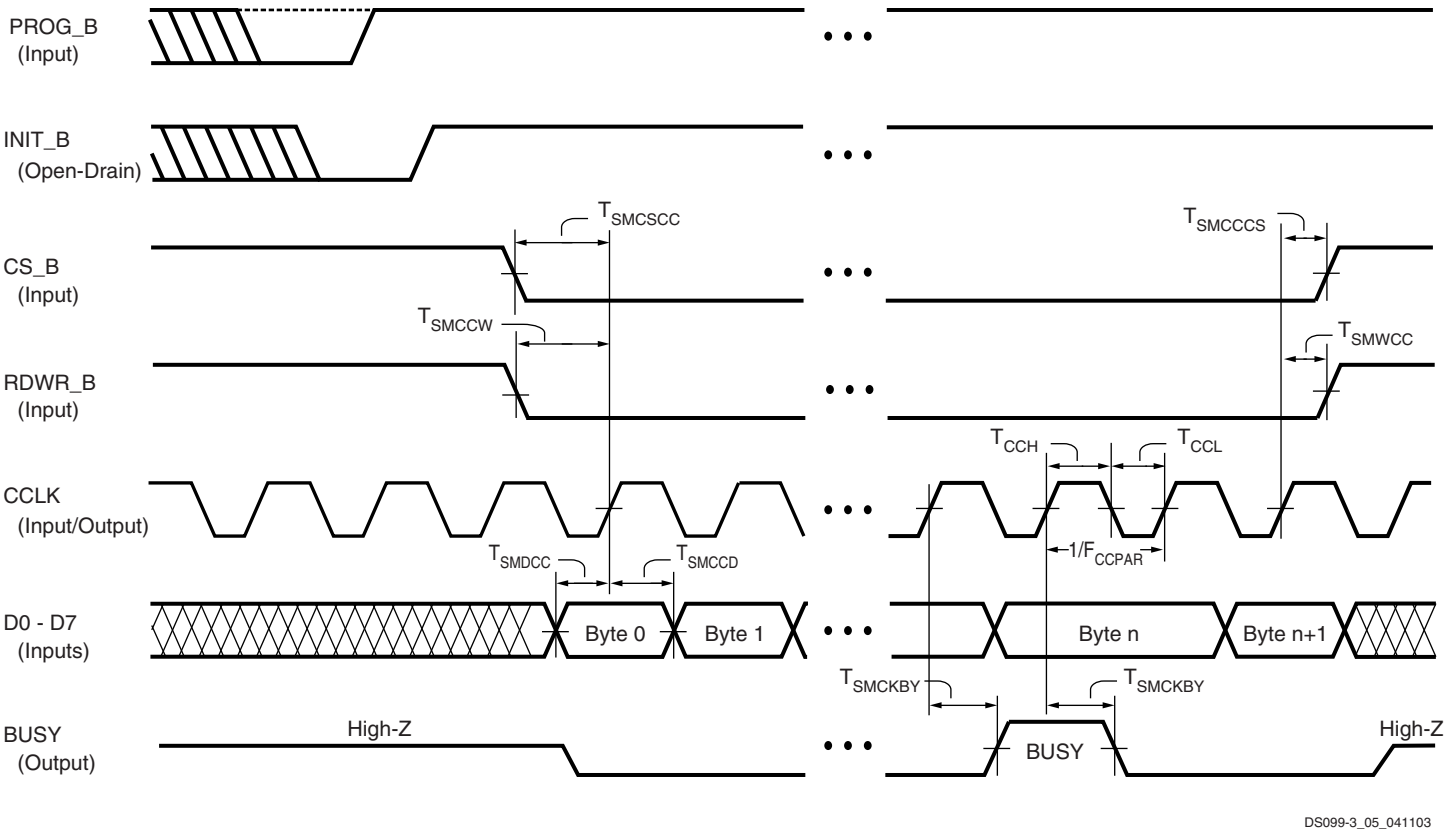

Figure 38: **Waveforms for Master and Slave Parallel Configuration**

Table 67: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/ Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	Slave	–	12.0	ns
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	10.0	–	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		10.0	–	ns
T_{SMCCW}(3)	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin		10.0	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	Both	0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin		0	–	ns
T_{SMWCC}(3)	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns

XC3S100E-4VQ100GI	2001+	BGA	2315
XC3S100E-4VQ100GC	2001+	BGA	2315
XC3S100E-4VQ100C	2001+	TQFP100	2315
XC3S100E-4VQ100	2001+	BGA	2315
XC3S100E-4VQ(G)100I	2001+	AA	2315
XC3S100E-4TQG144I	2001+	QFP144	2315
XC3S100E-4TQG144I	2001+	TQFP-144	2315
XC3S100E-4TQG144CS1	2001+	BGA	2315
XC3S100E-4TQG144C	2001+	TQFP144	2315
XC3S100E-4TQG144C	2001+	QFP144	2315
XC3S100E-4TQG144C	2001+	TQFP	2315
XC3S100E-4TQG144	2001+	TQFP	2315
XC3S100E-4TQG100I	2001+	QFP144	2315
XC3S100E-4TQ144I	2001+	QFP144	2315
XC3S100E-4TQ144GI	2001+	BGA	2315
XC3S100E-4TQ144GC	2001+	BGA	2315
XC3S100E-4TQ144C	2001+	TQFP144	2315
XC3S100E-4TQ144	2001+	BGA	2315
XC3S100E4TQ144	2001+	QFP144	2315
XC3S100E-4PQG208I	2001+	BGA	2315
XC3S100E-4PQG208C	2001+	BGA	2315
XC3S100E-4PQ208I	2001+	BGA	2315
XC3S100E-4PQ208GI	2001+	BGA	2315
XC3S100E-4PQ208GC	2001+	BGA	2315
XC3S100E-4PQ208C	2001+	BGA	2315
XC3S100E-4FTG256I	2001+	BGA	2315
XC3S100E-4FTG256C	2001+	BGA	2315
XC3S100E-4FT256I	2001+	BGA	2315
XC3S100E-4FT256GI	2001+	BGA	2315
XC3S100E-4FT256GC	2001+	BGA	2315
XC3S100E-4FT256C	2001+	BGA	2315
XC3S100E-4FGG484I	2001+	BGA	2315
XC3S100E-4FGG484C	2001+	BGA	2315
XC3S100E-4FGG400I	2001+	BGA	2315
XC3S100E-4FGG400C	2001+	BGA	2315
XC3S100E-4FGG320I	2001+	BGA	2315
XC3S100E-4FGG320C	2001+	BGA	2315
XC3S100E-4FG484I	2001+	BGA	2315
XC3S100E-4FG484GI	2001+	BGA	2315
XC3S100E-4FG484GC	2001+	BGA	2315
XC3S100E-4FG484C	2001+	BGA	2315

芯片详细信息

Manufacturer Part Number: XC2VP2-7FG456I	Pbfree Code: No	Rohs Code: No	Part Life Cycle Code: Obsolete
Ihs Manufacturer: XILINX INC	Part Package Code: BGA	Package Description: 1 MM PITCH, FBGA-456	Pin Count: 456
Reach Compliance Code: not_compliant	Manufacturer: Xilinx	Risk Rank: 5.82	Clock Frequency-Max: 1350 MHz
Combinatorial Delay of a CLB-Max: 0.28 ns	JESD-30 Code: S-PBGA-B456	JESD-609 Code: e0	Length: 23 mm
Moisture Sensitivity Level: 3	Number of CLBs: 352	Number of Inputs: 156	Number of Logic Cells: 3168
Number of Outputs: 156	Number of Terminals: 456	Organization: 352 CLBS	Package Body Material: PLASTIC/EPOXY
Package Code: BGA	Package Equivalence Code: BGA456,22X22,40	Package Shape: SQUARE	Package Style: GRID ARRAY
Peak Reflow Temperature (Cel): 225	Power Supplies: 1.5,1.5/3.3,2/2.5,2.5 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified
Seated Height-Max: 2.6 mm	Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.575 V	Supply Voltage-Min: 1.425 V
Supply Voltage-Nom: 1.5 V	Surface Mount: YES	Technology: CMOS	Terminal Finish: Tin/Lead (Sn63Pb37)
Terminal Form: BALL	Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 30
Width: 23 mm			