Chapter 4

User Primitives

The following configuration primitives are provided for users to access FPGA configuration resources during or after FPGA configuration.

BSCAN_VIRTEX5

JTAG is a standard four-pin interface: TCK, TMS, TDI, and TDO. Many applications are built around this interface. The JTAG TAP controller is a dedicated state machine inside the configuration logic. BSCAN_VIRTEX5 provides access between the JTAG TAP controller and user logic in fabric. There are up to four instances of BSCAN_VIRTEX5 for each device, each instance is controlled with the JTAG_CHAIN parameter. Table 4-1 lists the BSCAN_VIRTEX5 fabric pins.

Table 4-1: **BSCAN_VIRTEX5 Pin Table**

Pin Name	Type	Description
SEL	Output	Active-High interface selection output. SEL = 1 when the JTAG instruction register holds the corresponding USER1-4 instruction. Change in Update_IR state. SEL changes on the falling edge of TCK in the UPDATE_IR state of the TAP controller.
RESET	Output	Active-High reset output. RESET = 1 during the TEST-LOGIC-RESET state, PROGRAM_B, or during power up. This signal is deasserted on the falling edge of TCK.
TDI	Output	Fed through directly from the FPGA TDI pin.
DRCK	Output	DRCK is the same as TCK in the Capture_DR and Shift_DR states. If the interface is not selected by the instruction register, DRCK remains High.
CAPTURE	Output	Active-High pulse indicating the Capture_DR state. This signal is asserted on the falling edge of TCK.
UPDATE	Output	Active-High pulse indicating the Update_DR state. This signal is asserted on the falling edge of TCK.
SHIFT	Output	Active-High pulse indicating the Shift_DR state. This signal is asserted on the falling edge of TCK.
TDO	Input	TDO input driven from the user fabric logic. This signal is internally sampled on the falling edge before being driven out to the FPGA TDO pin.

CAPTURE_VIRTEX5

The CAPTURE_VIRTEX5 primitive is used to capture I/O, CLB, and block RAM output flip-flop status, and then read back through the configuration interface. The CAP input is sampled by CLK to generate an internal gcap signal. The I/O and CLB flip-flop status are captured into an FPGA configuration memory cell when the gcap signal is High. There are operation modes, a one-shot mode, or a continuous mode.

In one-shot mode, after the first CAP falling edge, gcap is held to 0 to avoid further capturing. An explicit RCAP command is required to re-arm the capture circuit.

In continuous mode, the CAP input is simply sampled by CLK, and becomes the gcap signal, allowing the user to control when to capture.

CAPTURE_VIRTEX5 should not operate simultaneously with the FRAME_ECC_VIRTEX5 primitive or the Readback CRC function (see Chapter 9, "Readback CRC") because capturing a value into configuration memory might cause a false error.

Table 4-2: **CAPTURE_VIRTEX5 Pin Table**

Pin Name	Type	Description
CLK	Input	Clock for sampling the CAP input.
CAP	Input	Active-High capture enable. The CAP input is sampled by the rising edge of CLK.

ICAP_VIRTEX5

The ICAP_VIRTEX5 primitive works the same way as the SelectMAP configuration interface except it is on the fabric side, and ICAP has a separate read/write bus, as opposed to the bidirectional bus in SelectMAP. The general SelectMAP timing diagrams and the SelectMAP bitstream ordering information as described in the "SelectMAP Configuration Interface" section of this user guide are also applicable to ICAP. It allows the user to access configuration registers, readback configuration data, or partially reconfigure the FPGA after configuration is done.

ICAP has three data width selections through the ICAP WIDTH parameter: x8, x16, and x32.

The two ICAP ports cannot be operated simultaneously. The design must start from the top ICAP, then switch back and forth between the two.

Table 4-3: **ICAP_VIRTEX5 Pin Table**

Pin Name	Type	Description
CLK	Input	ICAP interface clock
CE	Input	Active-Low ICAP interface select. Equivalent to CS_B in the SelectMAP interface.
WRITE	Input	0=WRITE, 1=READ. Equivalent to the RDWR_B signal in the SelectMAP interface.
I[31:0]	Input	ICAP write data bus. The bus width depends on ICAP_WIDTH parameter. The bit ordering is identical to the SelectMAP interface. See SelectMap Data Ordering in Figure 2-19.

Table 4-3: **ICAP_VIRTEX5 Pin Table *(Continued)***

Pin Name	Type	Description
O[31:0]	Output	Unregistered ICAP read data bus. The bus width depends on the ICAP_WIDTH parameter. The bit ordering is identical to the SelectMAP interface. See SelectMap Data Ordering in Figure 2-19.
BUSY	Output	Active-High busy status. Only used in read operations. BUSY remains Low during writes.

FRAME_ECC_VIRTEX5

The Virtex-5 Frame error correction code (ECC) logic is designed to detect single- or double-bit errors in configuration frame data. It uses SECDED (Hamming code) parity values based on the frame data generated by BitGen. During readback, the Frame ECC logic calculates a *syndrome* value using all the bits in the frame, including the ECC bits. If the bits have not changed from the original programmed values, then the syndrome bits are all 0s. If a single bit has changed, including any of the ECC bits, then the location of the bit is indicated by syndrome bits 10:0 and the syndrome bit 11 is 1. If two bits have changed, then syndrome bit 11 is 0 and the remaining bits are non-zero and meaningless. If more than two bits have changed, then the syndrome bits is indeterminate. The *error* output of the block is asserted if one or two bits have changed, indicating that action needs to be taken.

To use the Frame ECC logic, FRAME_ECC_VIRTEX5 must be instantiated in the user's design, and readback must be performed through SelectMAP, JTAG, or ICAP. At the end of each frame of readback, the *syndrome_valid* signal is asserted for one cycle of the readback clock (CCLK, TCK, or ICAP_CLK). The number of cycles required to read back a frame varies with the interface used. Refer to "Readback and Configuration Verification" in Chapter 7 for further information.

The FRAME_ECC_VIRTEX5 logic does not repair changed bits; this requires a user design. The design must be able to store at least one frame of data, or be able to fetch original frames of data for reload. A single frame is 1,312 bits. Following is an example of a simple repair implementation:

1. A frame is read out through ICAP and stored in block RAM. The frame address must be generated as each frame is read.
2. If an error is indicated by the *error* output of the FRAME_ECC block, then the readback is halted and the syndrome value is saved. If bit 11 is 0, then the whole frame must be restored. If bit 11 is 1, then bits 10:0 are used to locate the error bit in the saved frame, and the bit is inverted.
3. The repaired frame is then written back into the frame address generated in step 1.
4. Readback then begins again with the next frame address.

芯片详细信息

Manufacturer Part Number: XC2VP2-7FG456C	Pbfree Code: No	Rohs Code: No	Part Life Cycle Code: Obsolete
Ihs Manufacturer: XILINX INC	Part Package Code: BGA	Package Description: BGA, BGA456,22X22,40	Pin Count: 456
Reach Compliance Code: not_compliant	ECCN Code: EAR99	HTS Code: 8542.39.00.01	Manufacturer: Xilinx
Risk Rank: 5.81	Clock Frequency-Max: 1350 MHz	Combinatorial Delay of a CLB-Max: 0.28 ns	JESD-30 Code: S-PBGA-B456
JESD-609 Code: e0	Length: 23 mm	Moisture Sensitivity Level: 3	Number of CLBs: 352
Number of Inputs: 156	Number of Logic Cells: 3168	Number of Outputs: 156	Number of Terminals: 456
Operating Temperature-Max: 85 °C	Organization: 352 CLBS	Package Body Material: PLASTIC/EPOXY	Package Code: BGA
Package Equivalence Code: BGA456,22X22,40	Package Shape: SQUARE	Package Style: GRID ARRAY	Peak Reflow Temperature (Cel): 225
Power Supplies: 1.5,1.5/3.3,2/2.5,2.5 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified	Seated Height-Max: 2.6 mm
Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.575 V	Supply Voltage-Min: 1.425 V	Supply Voltage-Nom: 1.5 V
Surface Mount: YES	Technology: CMOS	Temperature Grade: OTHER	Terminal Finish: Tin/Lead (Sn63Pb37)
Terminal Form: BALL	Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature-Max (s): 30
Width: 23 mm			

XC3S100E-4FG400GI	2001+	BGA	2315
XC3S100E-4FG400GC	2001+	BGA	2315
XC3S100E-4FG400C	2001+	BGA	2315
XC3S100E-4FG320I	2001+	BGA	2315
XC3S100E-4FG320GI	2001+	BGA	2315
XC3S100E-4FG320GC	2001+	BGA	2315
XC3S100E-4FG320C	2001+	BGA	2315
XC3S100E-4CPG132I	2001+	BGA132	2315
XC3S100E-4CPG132C	2001+	BGA132	2315
XC3S100E-4CPG132C	2001+	BGA132	2315
XC3S100E-4CP132I	2001+	BGA-132	2315
XC3S100E-4CP132GI	2001+	BGA	2315
XC3S100E-4CP132GC	2001+	BGA	2315
XC3S100E-4CP132C	2001+	BGA	2315
XC3S100E-4CP132	2001+	BGA	2315
XC3S100E_06	2001+	BGA	2315
XC3S100E	2001+	TQFP144	2315
XC3S100-5TQ144C	2001+	QFP	2315
XC3S100-5TQ144	2001+	QFP	2315
XC3S100-5FG456C	2001+	BGA	2315
XC3S100-4FTG256C	2001+	BGA	2315
XC3S100-4FGG456C	2001+	BGA	2315
XC3S100-4FGG320C	2001+	BGA	2315
XC3S100-4FG456I	2001+	BGA	2315
XC3S1000L-4FT256C	2001+	BGA	2315
XC3S1000L-4FT256	2001+	BGA	2315
XC3S1000L-4FGG676C	2001+	BGA	2315
XC3S1000L-4FGG456C	2001+	BGA	2315
XC3S1000L-4FGG320C	2001+	BGA	2315
XC3S1000L-4FG676C	2001+	QFP	2315
XC3S1000L-4FG456C	2001+	BGA	2315
XC3S1000L-4FG320C	2001+	BGA	2315
XC3S1000L	2001+	BGA	2315
XC3S1000J-5FT256C	2001+	BGA	2315
XC3S1000J-5FG676C	2001+	BGA	2315
XC3S1000J-4FT256C	2001+	BGA	2315
XC3S1000J-4FG676C	2001+	BGA	2315
XC3S1000J-4FG456C	2001+	BGA	2315
XC3S1000J FT256ALQ	2001+	BGA	2315
XC3S1000FTG256EGQ-4C	2001+	BGA	2315
XC3S1000-FTG256EGQ	2001+	BGA	2315