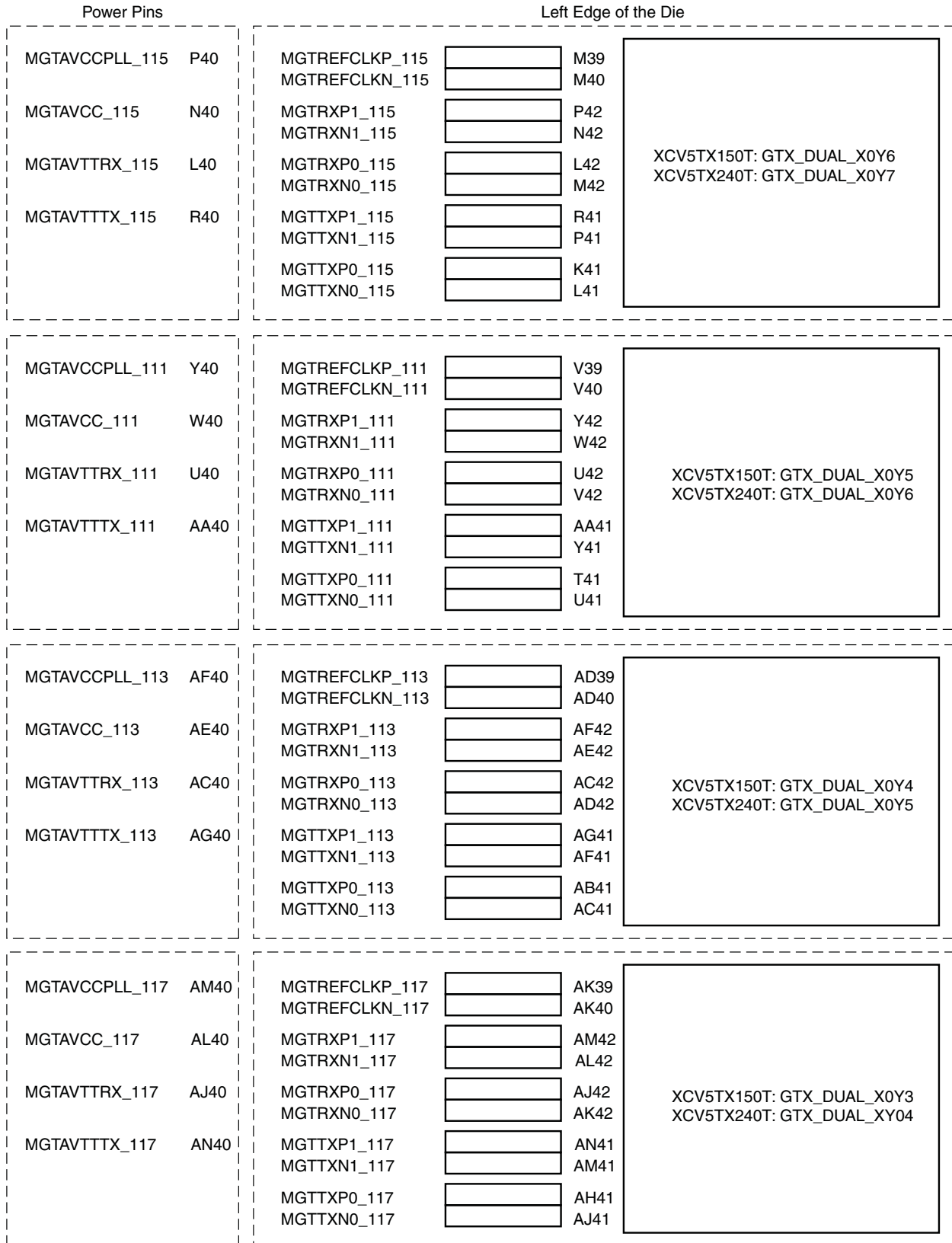


Table 1-5: GTX_DUAL Attribute Summary (Cont'd)

Attribute	Type	Description	Section (Page)
CLK25_DIVIDER	Integer	Sets the divider used to divide CLKIN down to an internal rate close to 25 MHz.	Clocking (page 98), Power Control (page 111)
CLKINDC_B	Boolean	Must be set to TRUE. Oscillators driving the dedicated reference clock inputs must be AC coupled.	Clocking (page 98), Analog Design Guidelines (page 254)
CLKRCV_TRST	Boolean	When set to TRUE, switches on the differential clock input pair's internal termination resistors.	Clocking (page 98), Analog Design Guidelines (page 254)
CM_TRIM_0 CM_TRIM_1	2-bit Binary	Adjusts the input common mode values.	RX Termination and Equalization (page 163)
COM_BURST_VAL_0[3:0] COM_BURST_VAL_1[3:0]	4-bit Binary	Number of bursts transmitted for a SATA COM sequence.	TX Out-of-Band/Beacon Signaling (page 158)
COMMA_10B_ENABLE_0 COMMA_10B_ENABLE_1	10-bit Binary	Sets which bits of MCOMMA/PCOMMA must be matched to incoming data and which bits are don't cares.	Configurable Comma Alignment and Detection (page 193)
COMMA_DOUBLE_0 COMMA_DOUBLE_1	Boolean	When TRUE, a PCOMMA match followed immediately by an MCOMMA match is required for comma detection. Used to detect A1/A2 framing characters for SONET.	Configurable Comma Alignment and Detection (page 193)
DEC_MCOMMA_DETECT_0 DEC_MCOMMA_DETECT_1	Boolean	Enables detection of negative 8B/10B commas.	Configurable 8B/10B Decoder (page 201)
DEC_PCOMMA_DETECT_0 DEC_PCOMMA_DETECT_1	Boolean	Enables detection of positive 8B/10B commas.	Configurable 8B/10B Decoder (page 201)
DEC_VALID_COMMA_ONLY_0 DEC_VALID_COMMA_ONLY_1	Boolean	Limits the set of commas to which RXCHARISCOMMA responds.	Configurable 8B/10B Decoder (page 201)
DFE_CAL_TIME	5-bit Binary	DFE calibration time.	Decision Feedback Equalization (page 168)
DFE_CFG_0[9:0] DFE_CFG_1[9:0]	10-bit Binary	DFE configuration settings.	Decision Feedback Equalization (page 168)
GEARBOX_ENDEC_0 GEARBOX_ENDEC_1	3-bit Binary	Selects Gearbox mode.	TX Gearbox (page 135), RX Gearbox (page 232)
MCOMMA_10B_VALUE_0 MCOMMA_10B_VALUE_1	10-bit Binary	Defines comma minus to raise RXCOMMADET and align the parallel data.	Configurable Comma Alignment and Detection (page 194)
MCOMMA_DETECT_0 MCOMMA_DETECT_1	Boolean	Set to TRUE to allow minus comma detection and alignment.	Configurable Comma Alignment and Detection (page 194)
OOB_CLK_DIVIDER	Integer	Sets the squelch clock rate based on CLKIN.	RX OOB/Beacon Signaling (page 175)



XC3S1000FGG676E	2001+	BGA	2315
XC3S1000FGG676	2001+	BGA	2315
XC3S1000-FGG456I	2001+	BGA456	2315
XC3S1000FGG456EGQ-4C	2001+	BGA	2315
XC3S1000-FGG456EGQ	2001+	BGA	2315
XC3S1000FGG456EGQ	2001+	BGA	2315
XC3S1000-FGG456C	2001+	BGA456	2315
XC3S1000FGG456	2001+	BGA	2315
XC3S1000-FGG320EGR4C	2001+	BGA	2315
XC3S1000-FG676EGQ	2001+	BGA	2315
XC3S1000FG676EGQ	2001+	BGA	2315
XC3S1000-FG676C	2001+	BGA	2315
XC3S1000FG676	2001+	BGA	2315
XC3S1000-FG456EGQ	2001+	BGA	2315
XC3S1000FG456EGQ	2001+	BGA	2315
XC3S1000FG456-4I	2001+	BGA	2315
XC3S1000-FG456-4C	2001+	BGA	2315
XC3S1000-FG456	2001+	BGA	2315
XC3S1000FG456	2001+	BGA	2315
XC3S1000FG320EGQ0621	2001+	BGA	2315
XC3S1000-FG320	2001+	BGA	2315
XC3S1000FG320	2001+	BGA	2315
XC3S1000F676	2001+	BGA	2315
XC3S1000F-4FT256L	2001+	BGA	2315
XC3S1000F256	2001+	BGA	2315
XC3S1000E-TQG144	2001+	QFP	2315
XC3S1000EFGG456	2001+	BGA	2315
XC3S1000E-FG320C	2001+	BGA	2315
xc3s1000e-4fgg320i	2001+	BGA	2315
XC3S1000BG456	2001+	BGA	2315
XC3S1000-8FG676C	2001+	BGA	2315
XC3S1000-6FTG256I	2001+	BGA	2315
XC3S1000-6FTG256C	2001+	BGA	2315
XC3S1000-6FT256C	2001+	BGA	2315
XC3S1000-6FGG676I	2001+	BGA	2315
XC3S1000-6FGG676C	2001+	BGA	2315
XC3S1000-6FGG456I	2001+	BGA	2315
XC3S1000-6FGG456C	2001+	BGA	2315
XC3S1000-6FGG320I	2001+	BGA	2315
XC3S1000-6FGG320C	2001+	BGA	2315
XC3S1000-6FG676I	2001+	QFP	2315



UG198_c4_15_071008

Figure 4-18: XCV5TX150T-FF1759 and XCV5TX240T-FF1759 GTX Placement (5 of 6)

芯片详细信息

Manufacturer Part Number: XC2VP2-7FG256I	Pbfree Code:  No	RoHS Code:  No	Part Life Cycle Code: Obsolete
Ihs Manufacturer: XILINX INC	Part Package Code: BGA	Package Description: 1 MM PITCH, FBGA-256	Pin Count: 256
Reach Compliance Code: not_compliant	Manufacturer: Xilinx	Risk Rank: 5.83	Clock Frequency-Max: 1350 MHz
Combinatorial Delay of a CLB-Max: 0.28 ns	JESD-30 Code: S-PBGA-B256	JESD-609 Code: e0	Length: 17 mm
Moisture Sensitivity Level: 3	Number of CLBs: 352	Number of Inputs: 140	Number of Logic Cells: 3168
Number of Outputs: 140	Number of Terminals: 256	Organization: 352 CLBS	Package Body Material: PLASTIC/EPOXY
Package Code: BGA	Package Equivalence Code: BGA256,16X16,40	Package Shape: SQUARE	Package Style: GRID ARRAY
Peak Reflow Temperature (Cel): 225	Power Supplies: 1.5, 1.5/3.3, 2/2.5, 2.5 V	Programmable Logic Type: FIELD PROGRAMMABLE GATE ARRAY	Qualification Status: Not Qualified
Seated Height-Max: 2 mm	Subcategory: Field Programmable Gate Arrays	Supply Voltage-Max: 1.575 V	Supply Voltage-Min: 1.425 V
Supply Voltage-Nom: 1.5 V	Surface Mount: YES	Technology: CMOS	Terminal Finish: Tin/Lead (Sn63Pb37)
Terminal Form: BALL	Terminal Pitch: 1 mm	Terminal Position: BOTTOM	Time@Peak Reflow Temperature- Max (s): 30
Width: 17 mm			

Resetting the GTX_DUAL Tile

Each GTX_DUAL tile offers several ways to reset its subcomponents. [Table 5-8](#) shows all the different ways of resetting a GTX_DUAL tile, and the subcomponents that are affected by each type of reset.

Table 5-8: Available Resets Pins and the Components Reset by These Reset Pins

	Component	Configuration	GTXRESET	PLLPOWERDOWN (Falling Edge)	TXRESET0 TXRESET1	RXCDRRESET0 RXCDRRESET1	RXRESET0 RXRESET1	RXBUFRESET0 RXBUFRESET1	PRBSCNTRRESET0 PRBSCNTRRESET1
GTX-to-Board Interface	Termination Resistor Calibration	✓							
Shared Resources	Shared PMA PLL	✓	✓	✓					
	PLL Lock Detection	✓	✓	✓					
	Reset Control	✓	✓	✓					
	Power Control	✓	✓	✓					
	Clocking	✓	✓	✓					
	DRP	✓							
TX PCS	FPGA TX Interface	✓	✓	✓	✓				
	8B/10B Encoder	✓	✓	✓	✓				
	TX Buffer	✓	✓	✓	✓				
	PRBS Generator	✓	✓	✓	✓				
	Polarity Control	✓	✓	✓	✓				
TX PMA	PISO	✓	✓	✓					
	TX Pre-emphasis	✓	✓	✓					
	TX OOB & PCI	✓	✓	✓					
	TX Driver	✓	✓	✓					
RX PCS	FPGA RX Interface	✓	✓	✓		✓	✓		
	RX Elastic Buffer	✓	✓	✓		✓	✓	✓	
	RX Status Control	✓	✓	✓		✓	✓		
	8B/10B Decoder	✓	✓	✓		✓	✓		
	Comma Detect and Align	✓	✓	✓		✓	✓		
	RX LOS State Machine	✓	✓	✓		✓	✓		
	RX Polarity	✓	✓	✓		✓	✓		
	PRBS Checker	✓	✓	✓		✓	✓		✓
	5x Oversampler	✓	✓	✓		✓	✓		