STK8BA50-S

Digital Output 3-axis MEMS Accelerometer

Datasheet

Version – 1.0

2017/7/12

Sensortek Technology Corporation

1. OVERVIEW

Description

The STK8BA50-S is a ±2g/±4g/±8g, 3-axis linear accelerometer, with digital output (I^2C). It is a low profile capacitive MEMS sensor featuring, compensation for 0g offset and gain errors, and conversion to 10-bit digital values at user configurable samples per second. The device can be arranged for sensor data changes through the interrupt pins. The STK8BA50-S is available in a small 2.0 mm x 2.0 mm x 1.0 mm LGA package and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Feature

- Low Voltage Operation:
  - Supply Internal Domain Voltage: 2.4V~3.6V
  - I/O Voltage Range: 1.62V~3.6V
- ±2g/±4g±/8g dynamically selectable full-scale
- I^2C digital output interface
- 10 bit data output
- 10000 g high shock survivability
- 2.0 mm x 2.0 mm x 1.0 mm LGA Package
- Configurable Samples from 14 to 2000 samples per second
- On-chip Interrupt-signal generator for New data
- RoHS Compliant
- Halogen Free
- Environmentally Preferred Product
- Moisture Sensitivity Level 3

Applications

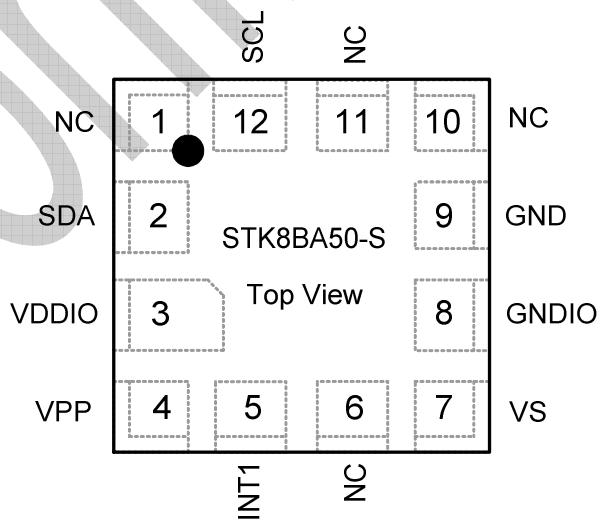
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation

2. PIN DESCRIPTION

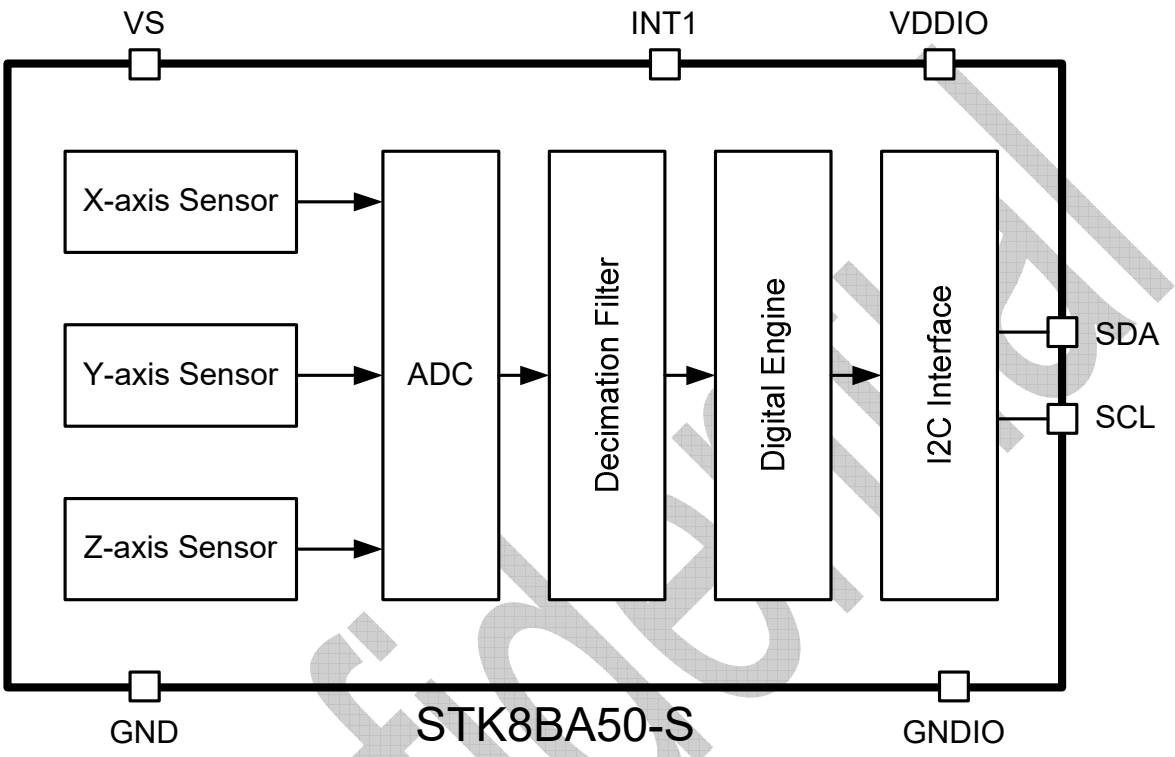
Pin#	Name	Dir.	Function
1	NC	NC	Not Internally Connected.
2	SDA	B	Serial Data (I^2C, Open-Drain)
3	VDDIO	PWR	Digital Interface Supply Voltage.
4	NC	NC	Recommended tie to GND.
5	INT1	O	Interrupt 1 Output.
6	NC	NC	Not Internally Connected.
7	VS	PWR	Supply Voltage.
8	GNDIO	GND	Must be connected to ground.
9	GND	GND	Must be connected to ground.
10	NC	NC	Not Internally Connected.
11	NC	NC	Not Internally Connected.
12	SCL	I	Serial Communications Clock (I^2C, Open-Drain)

Direction denotation:

O	Output	GND	Ground
I	Input	B	Bi-direction
PWR	Power	NC	Not Connected



3. FUNCTION BLOCK



4. ELECTRICAL SPECIFICATIONS

T_A = 25°C, VS = 2.6 V, VDDIO = 2.6 V, acceleration = 0 *g*, C_S = $C_{I/O}$ = 10 µF and 0.1 µF

Parameter	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Voltage Range (VS)		2.4	2.6	3.6	V
Interface Voltage Range (VDDIO)		1.62	2.6	3.6	V
Current consumption in normal mode			138		µA
Current consumption in suspend mode				1	µA
Digital high level input voltage (VIH)		0.7 x VDDIO			V
Digital low level input voltage (VIL)				0.3 x VDDIO	V
High level output voltage (VOH)[1]		0.8 x VDDIO			V
Low level output voltage (VOL)[1]				0.2 x VDDIO	V
OUTPUT DATA RATE AND BANDWIDTH	Each axis				
Bandwidth (BW)			7.81		Hz
			15.63		Hz
			31.25		Hz
			62.5		Hz
			125		Hz
			250		Hz
			500		Hz
			1000		Hz
Output data rate (ODR) in normal mode			BW * 2		Hz

1. IOL = 10mA, IOH = -4mA

5. MECHANICAL SPECIFICATIONS

T_A = 25°C, VS = 2.6 V, VDDIO = 2.6 V, acceleration = 0 *g*, C_S = $C_{I/O}$ = 10 µF and 0.1 µF

Parameter	Test Conditions	Min	Typ	Max	Unit
SENSOR INPUT	Each axis				
Measurement Range	User selectable		±2, ±4, ±8		g
Nonlinearity	Percentage of full scale		±0.5		%FS
Cross-Axis Sensitivity			1		%
OUTPUT RESOLUTION	Each axis				
±2 g Range	Full resolution		10		Bits
±4 g Range	Full resolution		10		Bits
±8 g Range	Full resolution		10		Bits
SENSITIVITY	Each axis				
Sensitivity at XOUT, YOUT, ZOUT	±2g, 10-bit resolution		256		LSB/g
	±4g, 10-bit resolution		128		LSB/g
	±8g, 10-bit resolution		64		LSB/g
Sensitivity Change Due to Temperature	X-, Y-, Z-Axes		±0.02		%/°C
0 g OFFSET[1]	Each axis				
0 g Output for XOUT, YOUT, ZOUT			±100		mg
0 g Offset Change Due to Temperature	X-, Y-, Z-Axes		±1		mg/°C
NOISE					
X-, Y-, Z-Axes	±2g, 10-bit resolution BW = 69 Hz		280		µg/sqrt(Hz)

1. These parameters are tested in production at final test, and could slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress.

6. ABSOLUTE MAXIMUM RATINGS

Symbol	Ratings	Maximum value	Unit
VS	Supply voltage	-0.3 to 3.6	V
VDDIO	Digital Interface Supply Voltage	-0.3 to 3.6	V
Vin	Input voltage on any control pin	-0.3 to 3.6	V
A_{UNP}	Acceleration (any axis, unpowered)	10000	g
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	4 (HBM)	kV
		500 (CDM)	V
		200 (MM)	V
		100 (Latch Up)	mA

7. DIGITAL INTERFACE

I^2C digital interface are available in STK8BA50-S.

7.1 I^2C

All registers in STK8BA50-S can be accessed via the I2C bus. All operations can be controlled by the related registers. There are two signals associated with the I2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional signal used for sending and receiving the data to/from the interface. Both signals are pull-up to $V_{DD\ I/O}$ through an external resistor.

A watchdog timer (WDT) is used to prevent the I^2C bus lock-up by STK8BA50-S. The I^2C bus will be reset and return to normal operation state once the WDT is reached. The WDT can be enabled/disabled by I2C_WDT_EN bit and the timer period can be set by I2C_WDT_SEL bit in register INTFCFG (0x34)

The STK8BA50-S I^2C command format description for reading and writing operation between the host and STK8BA50-S are shown in the following timing chart.

Slave Address

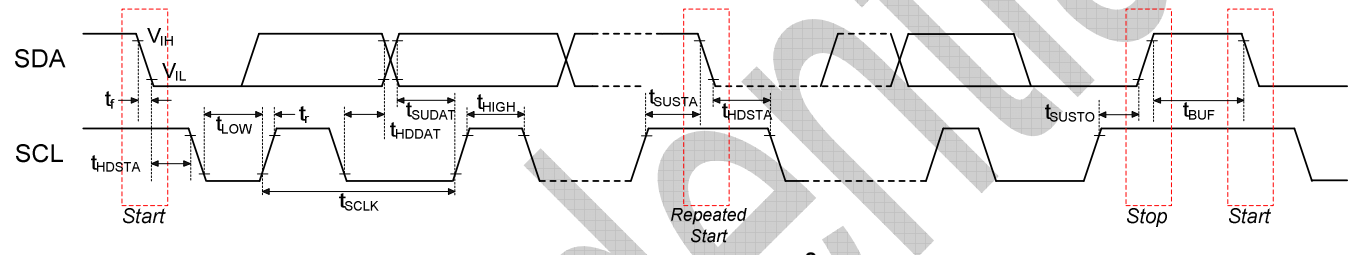
Slave Address (7-bit)	R/W Command Bit	OPERATION
0x18	0	Write Data to STK8BA50-S
	1	Read Data form STK8BA50-S

Characteristics of the I^2C Timing

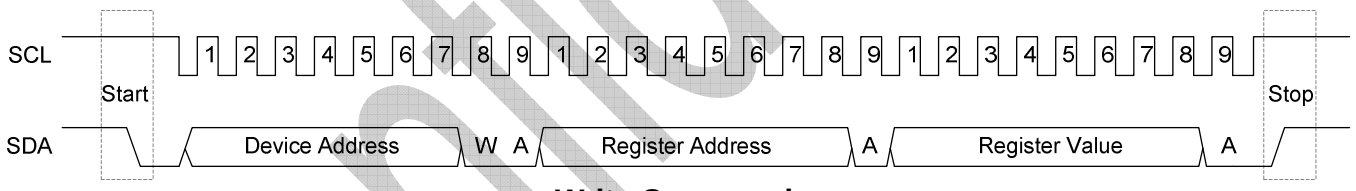
Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCLK}	SCL clock frequency	10	100	10	400	KHz
t_{HDSTA}	Hold time after (repeated) start condition. After this period, the first clock is generated	4.0	—	0.6	—	µs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	µs

t_{HIGH}	HIGH period of the SCL clock	4.0	—	0.6	—	μs
t_{SUSTA}	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
t_{HDDAT}	Data hold time	0	—	0	—	ns
t_{SUDAT}	Data set-up time	250	—	100	—	ns
t_r	Rise time of both SDA and SCL signals	—	1000	—	300	ns
t_f	Fall time of both SDA and SCL signals	—	300	—	300	ns
t_{SUSTO}	Set-up time for STOP condition	4.0	—	0.6	—	μs
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs

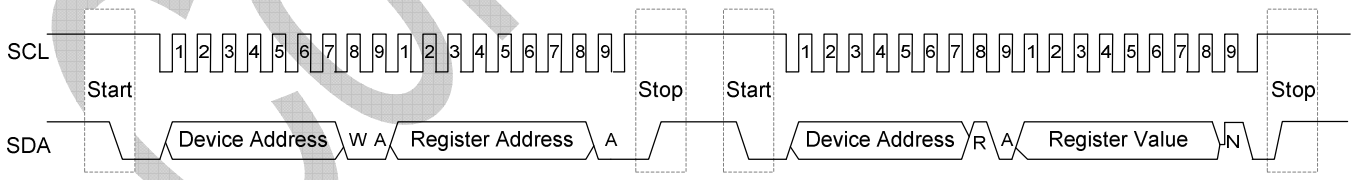
Note 1: f_{SCLK} is the $(t_{SCLK})^{-1}$.



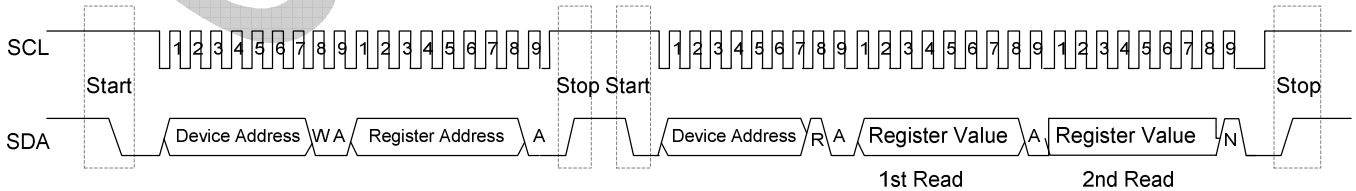
Timing Chart of the I²C



Write Command



Read Data



Sequential Read Data

8. PRINPICLE OF OPERATION

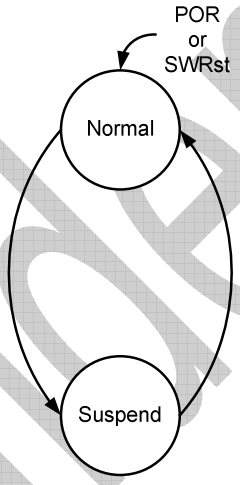
8.1 Mode of Operation

General Mode

STK8BA50-S acts as a slave and can communicate with a master(uC or uP). Acceleration data and status information can be accessed with I^2C interface. The interrupt pin are freely configured by user, depends on different requirement.

8.2 Power Management

STK8BA50-S has two different power modes, Normal Mode and Suspend Mode. After power-on, it will enter Normal Mode, and user could transfer to Suspend Mode for power-saving purpose.



In Normal Mode, all functions are available and data acquisition is performed continuously.

In Suspend Mode, whole analog and oscillator are power-down. No data acquisition is performed. Only register reading and writing to SUSPEND bit in register POWMODE (0x11) or register SWRST (0x14) are supported. Suspend mode can be entered by set SUSPEND bit in register POWMODE (0x11) to 1. In the suspend mode, the data does not auto clear and not updated but keeps the last value before entering into suspend mode.

8.3 Data, Range and BW

Acceleration Data

The acceleration data of STK8BA50-S is 10 bits and is given in two's complement format. The MSB in each axis will be stored in register XOUT2/YOUT2/ZOUT2 (0x03, 0x05, 0x07) individually, and the LSB will be stored in register XOUT1/YOUT1/ZOUT1 (0x02, 0x04, 0x06) individually. The NEW_X/NEW_Y/NEW_Z bit in register XOUT1/YOUT1/ZOUT1 (0x02, 0x04, 0x06) is used for new_data flag, and it will be set to 1 if the data is updated, and reset if either the corresponding MSB or LSB is read. Reading the acceleration data registers shall always start with the LSB part due to the data protection function. When data protection function is enabled, the content of an MSB register will be updated by reading the corresponding LSB register. The data protection function can be disabled (enabled) by writing '1' ('0') to the PROTECT_DIS bit in register DATASETUP (0x13). With disabled data protection, the content of both MSB and LSB registers is updated by a new value immediately.

Range

The STK8BA50-S supports four different acceleration measurement ranges. A measurement range can be selected by RANGE[3:0] bits in register RANGESEL (0x0F).

RANGE[3:0]	Sensing Range	Resolution
4'b0011	±2g	3.91 mg/LSB
4'b0101	±4g	7.81 mg/LSB
4'b1000	±8g	15.62 mg/LSB
others	undefined	undefined

Bandwidth

There are two different data stream of STK8BA50-S, unfiltered data and filtered data. Unfiltered data is sampled as 2kHz, and the sample rate of filtered data depends on the selected bandwidth; it is twice of the bandwidth. If the DATA_SEL bit in register DATASETUP (0x13) is set to '0' ('1') , the filtered (unfiltered) data will be stored in the XOUT/YOUT/ZOUT data register. Each of the data stream can be separately offset-compensated, and also can be the data source of interrupts controller. The actual bandwidth for the filtered data can be selected by BW[4:0] bits in register BWSEL (0x10).

BW[4:0]	Actual Bandwidth (Hz)
5'b00xxx	7.81
5'b01000	7.81
5'b01001	15.63
5'b01010	31.25
5'b01011	62.5
5'b01100	125
5'b01101	250
5'b01110	500
5'b01111	1000
5'b1xxxx	1000

8.4 Status and Interrupt Event Detection

The following table shows the interrupt event offered by STK8BA50-S. The INT pins are integrated for new data. If the condition of enabled new data interrupt is fulfilled, the corresponding status is set to '1' and selected INT pin is asserted.

Interrupt Event	Control Bit in Register INTEN1 (0x17)	Status Bit in Register INTSTS1 (0x0A)
New Data	DATA_EN	DATA_STS

Interrupt Mode

Both filtered and unfiltered data could be the data source of the new data interrupt. Setting the corresponding bit in register DATASRC (0x1E) to '0'('1'), filtered(unfiltered) data is selected as the source for related interrupt.

Interrupt Pin Mapping

The mapping of interrupts to the INT1 is controlled by registers INTMAP (0x1A). Setting the corresponding bit to '1'('0') maps(un-maps) the related interrupt to the INT1 pin

INT Pin Output Type and Active Level

INT1 could be configured as Push-Pull/Open-Drain output and the active level could also be set as active-high/active-low. The related bits in register INTCFG1 (0x20) are used to select the INT1 output type and active level.

8.5 Offset Compensation

Manual Compensation

STK8BA50-S offers the manual digital offset-compensation method. It is done by adding a compensation value to the acceleration data coming from the ADC. The registers OFSTX/Y/Z (0x38, 0x39, 0x3A) are used to for the offset compensation purpose and are given in two's complement format. 1 LSB of OFSTX/Y/Z represents 7.81 mg in any sensing range.

By writing '1' to the OFST_RST bit in register OFSTCOMP1 (0x36), all offset compensation registers are reset to zero.

It is recommended to write into these registers immediately after a new data interrupt in order not to disturb running offset computations.

9. REGISTER DEFINATION

ADDR	REG NAME	BIT 7	6	5	4	3	2	1	0	Default
00h	CHIP_ID	CHIP_ID[7:0]								86h
01h	RESERVED	reserved								00h
02h	XOUT1	XOUT[1:0]		reserved					NEW_X	00h
03h	XOUT2	XOUT[9:2]								00h
04h	YOUT1	YOUT[1:0]		reserved					NEW_Y	00h
05h	YOUT2	YOUT[9:2]								00h
06h	ZOUT1	ZOUT[1:0]		reserved					NEW_Z	00h
07h	ZOUT2	ZOUT[9:2]								00h
08h	RESERVED	reserved								00h
09h	RESERVED	reserved								00h
0Ah	INTSTS	DATA_STS	reserved							00h
0Bh-0Eh	RESERVED	reserved								00h
0Fh	RANGESEL	reserved				RANGE[3:0]				03h
10h	BWSEL	reserved			BW[4:0]					1Fh
11h	POWMODE	SUSPEND	reserved							00h
12h	RESERVED	reserved								00h
13h	DATASETUP	DATA_SEL	PROTECT_DIS	reserved						00h
14h	SWRST	SWRST[7:0]								00h
15h	RESERVED	reserved								00h
16h	RESERVED	reserved								00h
17h	INTEN	reserved			DATA_EN	reserved				00h
18h	RESERVED	reserved								00h
19h	RESERVED	reserved								00h
1Ah	INTMAP	reserved							DATA2INT1	00h
1Bh-1Dh	RESERVED	reserved								00h
1Eh	DATASRC	reserved		DATA_SRC	reserved					00h
1Fh	RESERVED	reserved								00h
20h	INTCFG1	reserved						INT1_OD	INT1_LV	01h
21h-33h	RESERVED	reserved								00h
34h	INTFCFG	reserved					I2C_WDT_EN	I2C_WDT_SEL	reserved	00h
35h	RESERVED	reserved								00h
36h	OFSTCOMP1	OFST_RST	reserved							00h
37h	RESERVED	reserved								00h
38h	OFSTX	OFST_X[7:0]								00h
39h	OFSTY	OFST_Y[7:0]								00h
3Ah	OFSTZ	OFST_Z[7:0]								00h

CHIP_ID Register (00h)

b7	b6	b5	b4	b3	b2	b1	b0
CHIP_ID[7:0]							
8'b10000110							
R							

XOUT1 Register (02h)

b7	b6	b5	b4	b3	b2	b1	b0
XOUT[1:0]		reserved					NEW_X
2'b00		2'b00000					0
R		R					R

XOUT2 Register (03h)

b7	b6	b5	b4	b3	b2	b1	b0
XOUT[9:2]							
8'b00000000							
R							

XOUT1/XOUT2 register contain the x-axis acceleration data and the new data flag for the x-axis.

YOUT1 Register (04h)

b7	b6	b5	b4	b3	b2	b1	b0
YOUT[1:0]		reserved					NEW_Y
2'b00		2'b00000					0
R		R					R

YOUT2 Register (05h)

b7	b6	b5	b4	b3	b2	b1	b0
YOUT[9:2]							
8'b00000000							
R							

YOUT1/YOUT2 register contain the y-axis acceleration data and the new data flag for the y-axis.

ZOUT1 Register (06h)

b7	b6	b5	b4	b3	b2	b1	b0
ZOUT[1:0]		reserved					NEW_Z
2'b00		2'b00000					0
R		R					R

ZOUT2 Register (07h)

b7	b6	b5	b4	b3	b2	b1	b0
ZOUT[9:2]							
8'b00000000							
R							

ZOUT1/ZOUT2 register contain the z-axis acceleration data and the new data flag for the z-axis.

INTSTS Register (0Ah)

b7	b6	b5	b4	b3	b2	b1	b0
DATA_STS	reserved						
0	2'b0000000						
R	R						

This register contains the new data interrupt status in STK8BA50-S.

BIT	BIT NAME	Description
7	DATA_STS	New data interrupt status.

RANGESEL Register (0Fh)

b7	b6	b5	b4	b3	b2	b1	b0
reserved				RANGE[3:0]			
2'b0000				4'b0011			
R				R/W			

This register contains the STK8BA50-S acceleration sensing range.

RANGE[3:0]	Sensing Range
4'b0011	±2g
4'b0101	±4g
4'b1000	±8g
others	undefined

BWSEL Register (10h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved			BW[4:0]				
2'b000			5'b11111				
R			R/W				

This register contains the output data bandwidth selection.

BW[4:0]	Actual Bandwidth (Hz)
5'b00xxx	7.81
5'b01000	7.81
5'b01001	15.63
5'b01010	31.25
5'b01011	62.5
5'b01100	125
5'b01101	250
5'b01110	500
5'b01111	1000
5'b1xxxx	1000

POWMODE Register (11h)

b7	b6	b5	b4	b3	b2	b1	b0
SUSPEND	reserved						
0	2'b0000000						
R/W	R						

This register contains the power mode selection.

BIT	BIT NAME	Description
7	SUSPEND	Suspend mode enable. 0 : suspend mode disable. 1 : suspend mode enable.

DATASETUP Register (13h)

b7	b6	b5	b4	b3	b2	b1	b0
DATA_SEL	PROTECT_DIS	reserved					
0	0	2'b000000					
R/W	R/W	R					

This register is used to select if the output data is filtered or unfiltered and how the output data contained in the register XOUT1/XOUT2, YOUT1/YOUT2, ZOUT1/ZOUT2 are updated.

BIT	BIT NAME	Description
6	PROTECT_DIS	0 : Enable the data protection function. 1 : Disable the data protection function.

7	DATA_SEL	0 : Data output filtered. 1 : Data output unfiltered.

SWRST Register (14h)

b7	b6	b5	b4	b3	b2	b1	b0
SWRST[7:0]							
8'b00000000							
W							

This register is used to software reset. Write 0xB6 into SWRST to reset all the registers to default value.

INTEN Register (17h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved			DATA_EN	reserved			
2'b000			0	2'b0000			
R			R/W	R			

This register contains the several interrupt enable bit.

BIT	BIT NAME	Description
4	DATA_EN	0 : Disable new data interrupt. 1 : Enable new data interrupt.

INTMAP Register (1Ah)

b7	b6	b5	b4	b3	b2	b1	b0
reserved							DATA2INT1
2'b0000000							0
R							R/W

This register is used to map the related interrupt to the desired INT pin.

BIT	BIT NAME	Description
0	DATA2INT1	0 : Do not map new data interrupt to INT1. 1 : Map new data interrupt to INT1.

DATASRC Register (1Eh)

b7	b6	b5	b4	b3	b2	b1	b0
reserved		DATA_SRC	reserved				
2'b00		0	2'b00000				
R		R/W	R				

This register is used to select the data source format for the related interrupt.

BIT	BIT NAME	Description
5	DATA_SRC	0 : Filtered data source is used for new data interrupt. 1 : Unfiltered data source is used for new data interrupt.

INTCFG1 Register (20h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved						INT1_OD	INT1_LV
2'b000000						0	1
R						R/W	R/W

This register is used to define the INT1 pin output type and active level. Open-drain or Push-pull output type and active high or active low can be selected for INT1 pin.

BIT	BIT NAME	Description
0	INT1_LV	INT1 active level selection. 0 : Active low. 1 : Active high.

1	INT1_OD	INT1 output type selection. 0 : Push-pull output type. 1 : Open-drain output type.

INTFCFG Register (34h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved					I2C_WDT_EN	I2C_WDT_SEL	reserved
2'b00000					0	0	0
R					R/W	R/W	R

This register contains the digital interface parameters for the I^2C interface.

BIT	BIT NAME	Description
1	I2C_WDT_SEL	I^2C watchdog timer period selection. 0 : Watchdog timer period 1ms. 1 : Watchdog timer period 50ms.
2	I2C_WDT_EN	I^2C watchdog timer enable bit. 0 : Disable I2C watchdog timer. 1 : Enable I2C watchdog timer.

OFSTCOMP1 Register (36h)

b7	b6	b5	b4	b3	b2	b1	b0
OFST_RST	reserved						
0	2'b0000000						
W	R						

This register is used to define the setting for the offset compensation.

BIT	BIT NAME	Description
7	OFST_RST	1 : Reset all the offset compensation register (register 0x38 ~ 0x3A) to zero.

OFSTX Register (38h)

B7	b6	b5	b4	b3	b2	b1	b0
OFST_X[7:0]							
8'b00000000							
R/W							

This register contains the offset compensation value for the x-axis data output.

OFSTY Register (39h)

B7	b6	b5	b4	b3	b2	b1	b0
OFST_Y[7:0]							
8'b00000000							
R/W							

This register contains the offset compensation value for the y-axis data output.

OFSTZ Register (3Ah)

b7	b6	b5	b4	b3	b2	b1	b0
OFST_Z[7:0]							
8'b00000000							
R/W							

This register contains the offset compensation value for the z-axis data output.

Register 0x38 to 0x3A can be modified manually set by user. The value in these register will be added to the actual acceleration data sensing by STK8BA50-S and store the new value to XOUT/YOUT/ZOUT register.

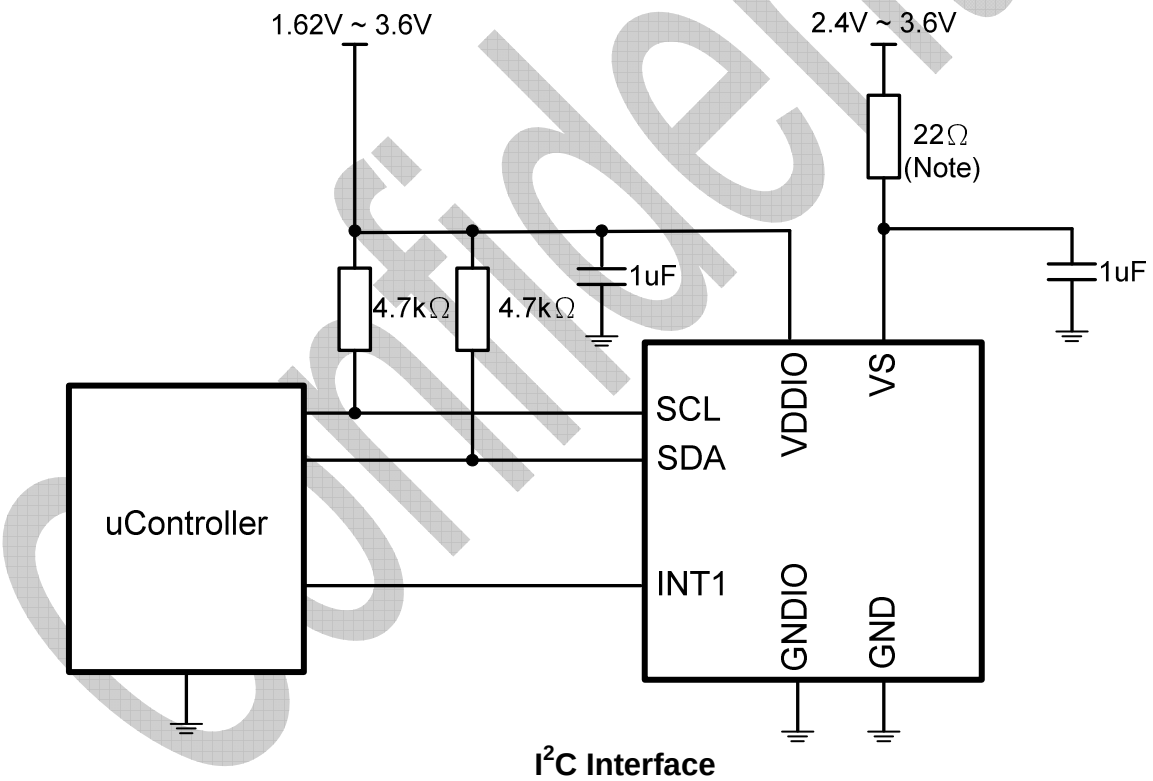
10. APPLICATION INFORMATION

10.1 New Data Interrupt

This interrupt serves for synchronous reading of acceleration data. It is generated after storing a new value of z-axis acceleration data in the data register. The interrupt is cleared automatically when the next cycle of data acquisition starts. The interrupt status is '0' for at least 50μs.

Control Register	Bit Name	Function
INTEN[4]	DATA_EN	'1': enabled, '0': disabled, and the interrupt mode is fixed to non-latched.
INTSTS[7]	DATA_STS	The interrupt status
INTMAP[0]	DATA2INT1	New data interrupt maps to INT1.
DATASRC[5]	DATA_SRC	'1': unfiltered data, '0': filtered data, as the input of the new data interrupt

10.2 Application Circuit



I²C Interface

Note : A 22 Ohm resistor is recommended to filter out the system power noise.

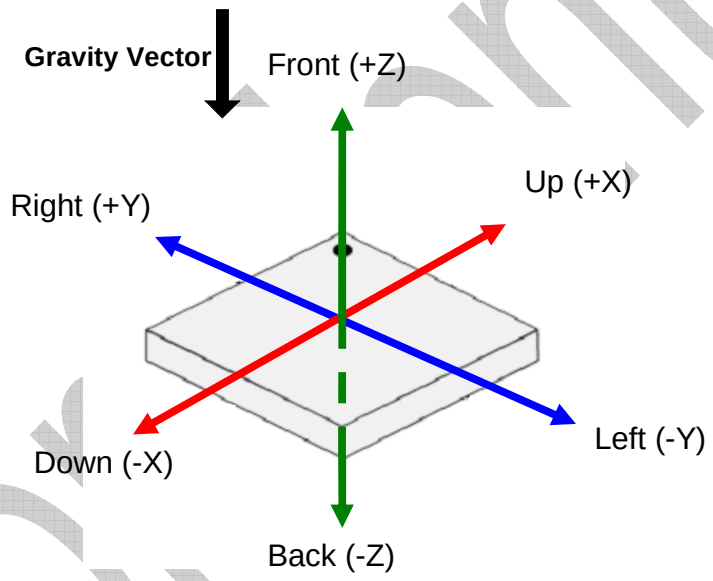
10.3 Sensing Axes Orientation

By measuring the acceleration components respect to g field, the position and orientation information could be recognized. It could be used for such applications as Portrait/Landscape in Mobile phone/PDA/PMP. This enables a product to set its display orientation appropriately to either portrait/landscape mode, or to turn off the display if the product is placed upside down. The sensor provides positive or negative directions of X/Y/Z axes. The relationship between directions and six different positions: Left, Right, Up, Down, Back, and Front, is shown in the following figure.

If the sensor is at rest and the force of gravity is acting along the indicated directions, the output of the corresponding channel will be negative (static acceleration).

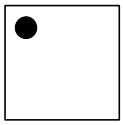
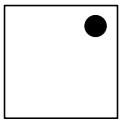
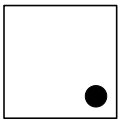
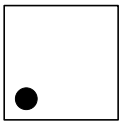
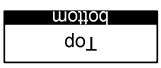
Example: If the sensor is at rest or at uniform motion in a gravity field according to the figure given below, the output signals are:

± 0g for the X-axis
± 0g for the Y-axis
+ 1g for the Z-axis



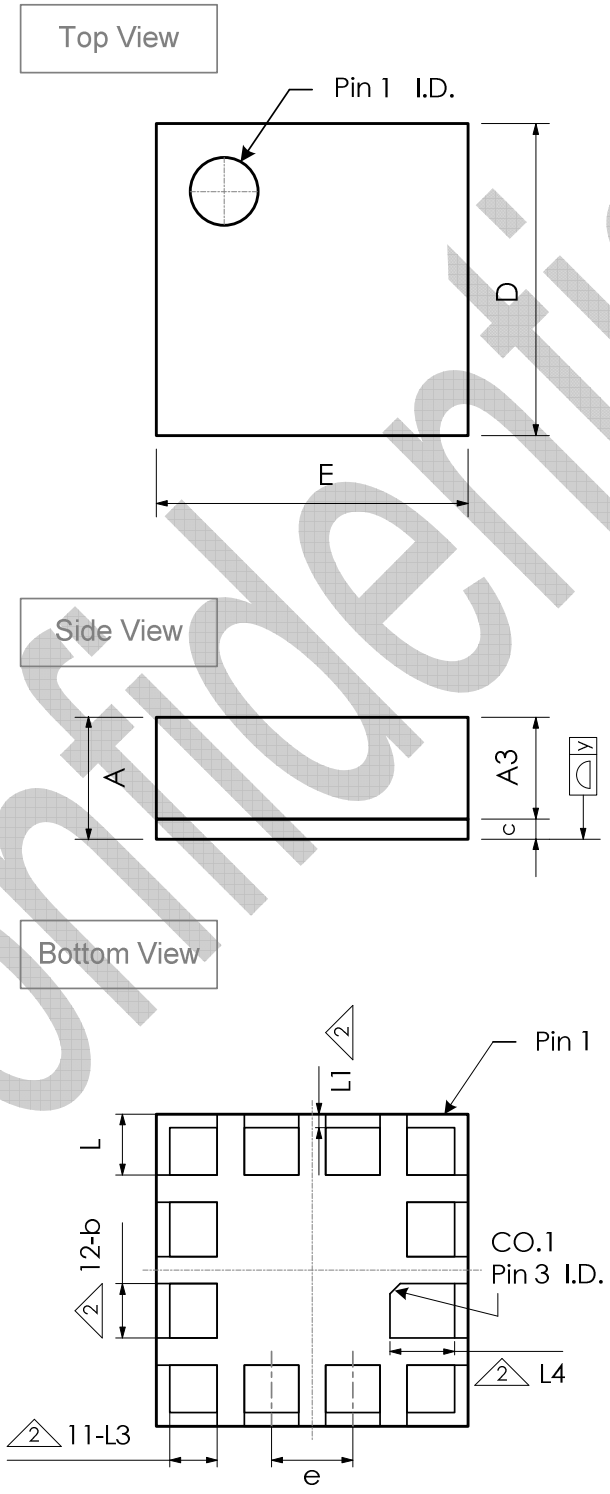
Sensing axes orientation

The following table lists all corresponding output signals on X, Y, and Z while the sensor is at rest or at uniform motion in a gravity field under assumption of a ±2g range setting, a 10 bit resolution, and a top down gravity vector as shown above.

Sensor Orientation & Gravity Vector	 Top View	 Top View	 Top View	 Top View	 Side View	 Side View
X-axis Output	+1g /256LSB	0g / 0 LSB	-1g/256 LSB	0g / 0 LSB	0g / 0 LSB	0g / 0 LSB
Y-axis Output	0g / 0 LSB	+1g/256 LSB	0g / 0 LSB	-1g/256 LSB	0g / 0 LSB	0g / 0 LSB
Z-axis Output	0g / 0 LSB	0g / 0 LSB	0g / 0 LSB	0g / 0 LSB	+1g/256 LSB	-1g/256 LSB

11. PACKAGE OUTLINE

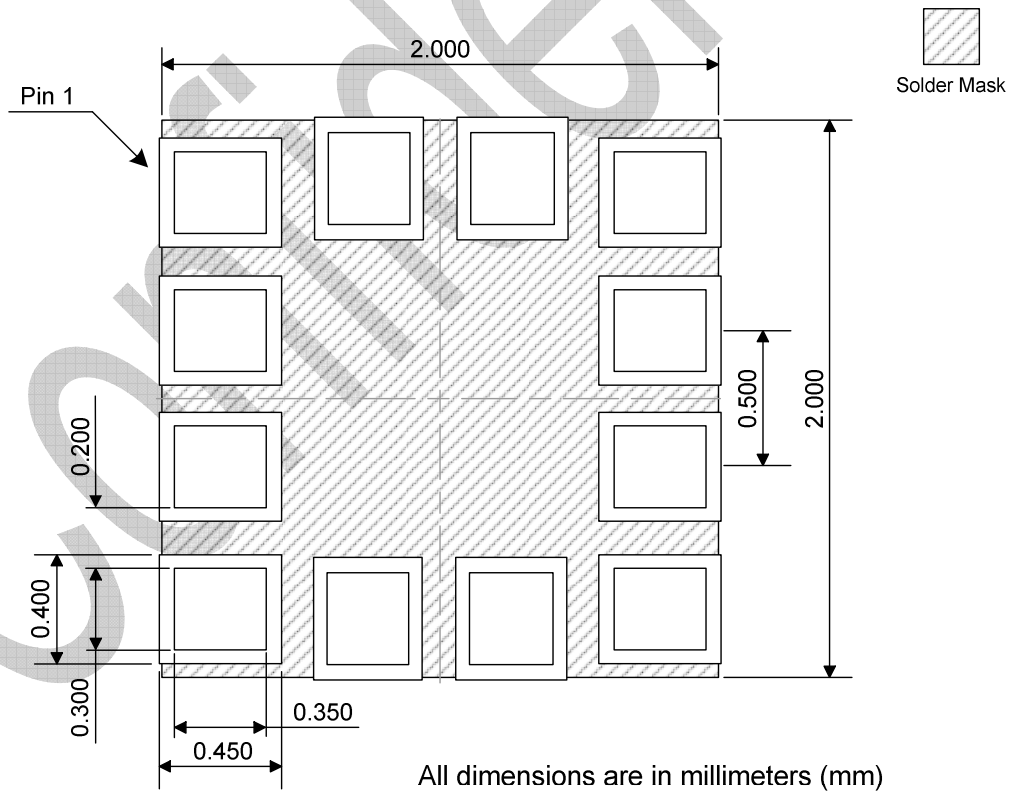
LGA Package Outline Drawing



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX
A	0.95	1.0	1.05
A3	---	0.82 REF.	---
b	0.23	0.28	0.33
c	---	0.18 REF.	---
D	1.90	2.00	2.10
E	1.90	2.00	2.10
e	---	0.50	---
L	0.325	0.375	0.425
L1	---	0.05	---
L3	0.275	0.325	0.375
L4	0.375	0.425	0.475
y	0.00	---	0.10

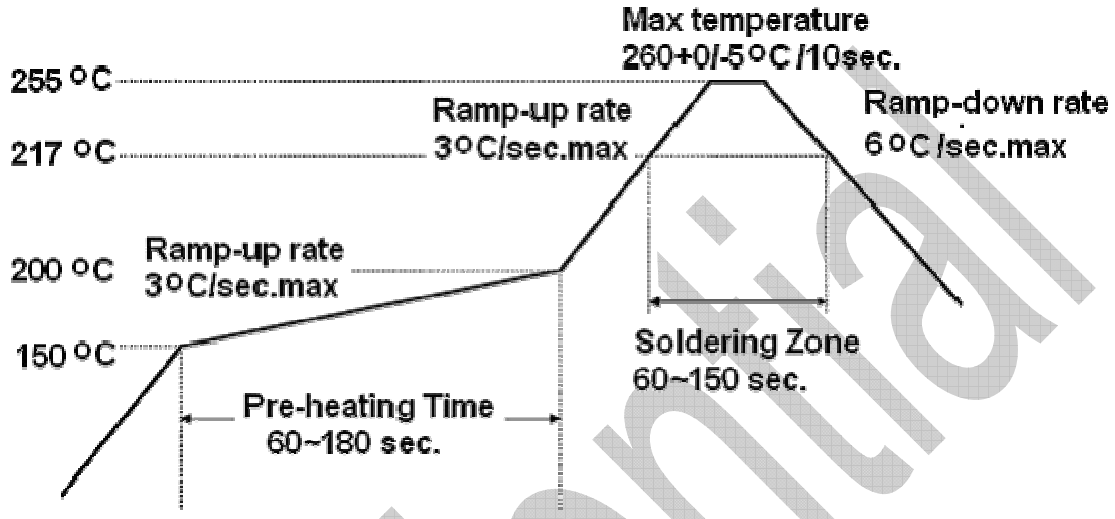
Recommended PCB Layout

The PCB layout should use NSMD (Non solder mask defined) pad definitions for all pads. The solder mask opening must be defined at least 0.05 mm larger than the metal pad on all sides.



11.1 Soldering Condition

1. Pb-free solder temperature profile.



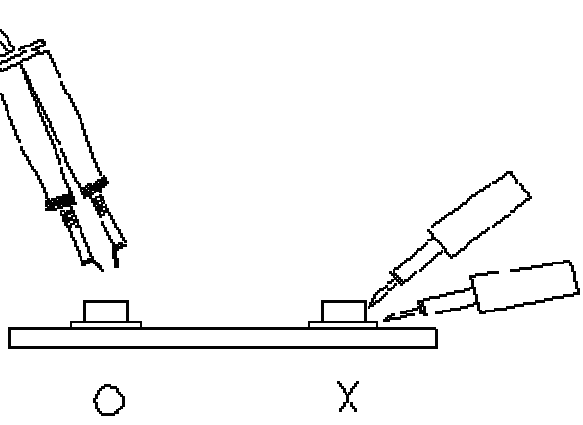
2. Reflow soldering should not be done more than three times.
3. When soldering, do not put stress on the ICs during heating.
4. After soldering, do not warp the circuit board.

11.2 Soldering Iron

Each terminal is to go to the tip of soldering iron temperature less than 350℃ for 3 seconds within once in less than the soldering iron capacity 25W. Leave two seconds and more intervals, and do soldering of each terminal. Be careful because the damage of the product is often started at the time of the hand solder.

11.3 Repairing

Repair should not be done after the ICs have been soldered. When repairing is unavoidable, a double-head soldering iron should be used (as below figure). It should be confirmed beforehand whether the characteristics of the ICs will or will not be damaged by repairing.



12. STORAGE INFORMATION

12.1 Storage Condition

1. Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.
2. The delivery product should be stored with the conditions shown below:

Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

12.2 Treatment After Unsealed

1. Floor life (time between soldering and removing from MBB) must not exceed the time shown below:

Floor Life	168 Hours
Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

2. When the floor life limits have been exceeded or the devices are not stored in dry conditions, they must be re-baked before reflow to prevent damage to the devices. The recommended conditions are shown below

Temperature	60℃
Re-Baking Time	12 Hours

Revision History

Date	Version	Modified Items
2017/07/12	1.0	Initial release.

