Async/Page/Burst CellularRAM™ 1.5

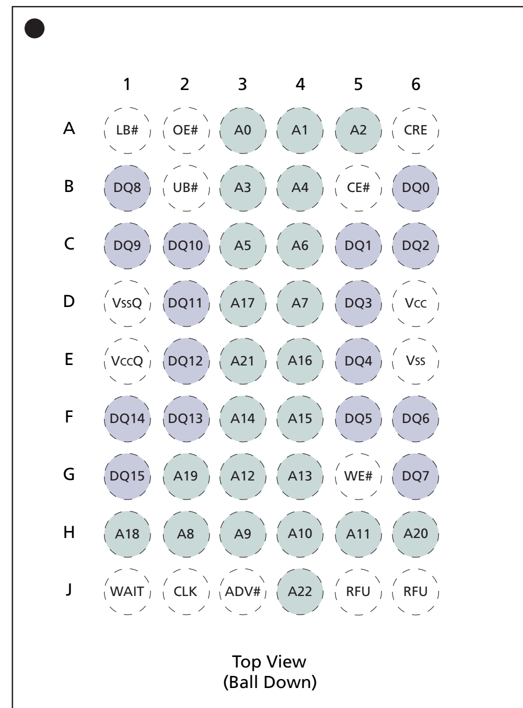
MT45W8MW16BGX

Features

- Single device supports asynchronous, page, and burst operations
- VCC, VCCQ voltages
  - 1.70–1.95V VCC
  - 1.7–3.6V[1] VCCQ
- Random access time: 70ns
- Burst mode READ and WRITE access
  - 4, 8, 16, or 32 words, or continuous burst
  - Burst wrap or sequential
  - MAX clock rate: 133 MHz (^tCLK = 7.5ns)
  - Burst initial latency: 35ns (5 clocks) at 133 MHz
  - ^tACLK: 5.5ns at 133 MHz
- Page mode READ access
  - Sixteen-word page size
  - Interpage READ access: 70ns
  - Intrapage READ access: 20ns
- Low power consumption
  - Asynchronous READ: <25mA
  - Intrapage READ: <15mA
  - Initial access, burst READ: (37.5ns [5 clocks] at 133 MHz) <45mA
  - Continuous burst READ: <40mA
  - Standby: <50µA (TYP at 25°C)
  - Deep power-down: <3µA (TYP)
- Low-power features
  - On-chip temperature-compensated refresh (TCR)
  - Partial-array refresh (PAR)
  - Deep power-down (DPD) mode

Options	Designator
• Configuration	
– 8 Meg x 16	MT45W8MW16B
– VCC core voltage: 1.70–1.95V	
– VCCQ I/O voltage: 1.7–3.6V[1]	
• Package	
– 54-ball VFBGA—“green”	GX
• Timing	
– 70ns access	–70
– 85ns access	–85

Figure 1: 54-Ball VFBGA Ball Assignment



Options (continued)	Designator
• Frequency	
– 66 MHz	6
– 80 MHz	8
– 104 MHz	1
– 133 MHz	13
• Standby power at 85°C	
– Standard: 200µA (MAX)	None
– Low power: 160µA (MAX)	L
• Operating temperature range	
– Wireless (–30°C to +85°C)	WT
– Industrial (–40°C to +85°C)	IT

Notes: 1. The 3.6V I/O and the 133MHz clock frequency exceed the CellularRAM 1.5 Workgroup specification.

Part Number Example:

MT45W8MW16BGX-7013LWT

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General Description

Micron® CellularRAM™ is a high-speed, CMOS pseudo-static random access memory developed for low-power, portable applications. The MT45W8MW16BGX device has a 128Mb DRAM core, organized as 8 Meg x 16 bits. These devices include an industry-standard burst mode Flash interface that dramatically increases read/write bandwidth compared with other low-power SRAM or pseudo-SRAM offerings.

To operate seamlessly on a burst Flash bus, CellularRAM products incorporate a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three mechanisms to minimize standby current. Partial-array refresh (PAR) enables the system to limit refresh to only that part of the DRAM array that contains essential data. Temperature-compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature—the refresh rate decreases at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) enables the system to halt the refresh operation altogether when no vital information is stored in the device. The system-configurable refresh mechanisms are accessed through the RCR.

This CellularRAM device is compliant with the industry-standard CellularRAM 1.5 feature set established by the CellularRAM Workgroup. It includes support for both variable and fixed latency, with three output-device drive-strength settings, additional wrap options, and a device ID register (DIDR).

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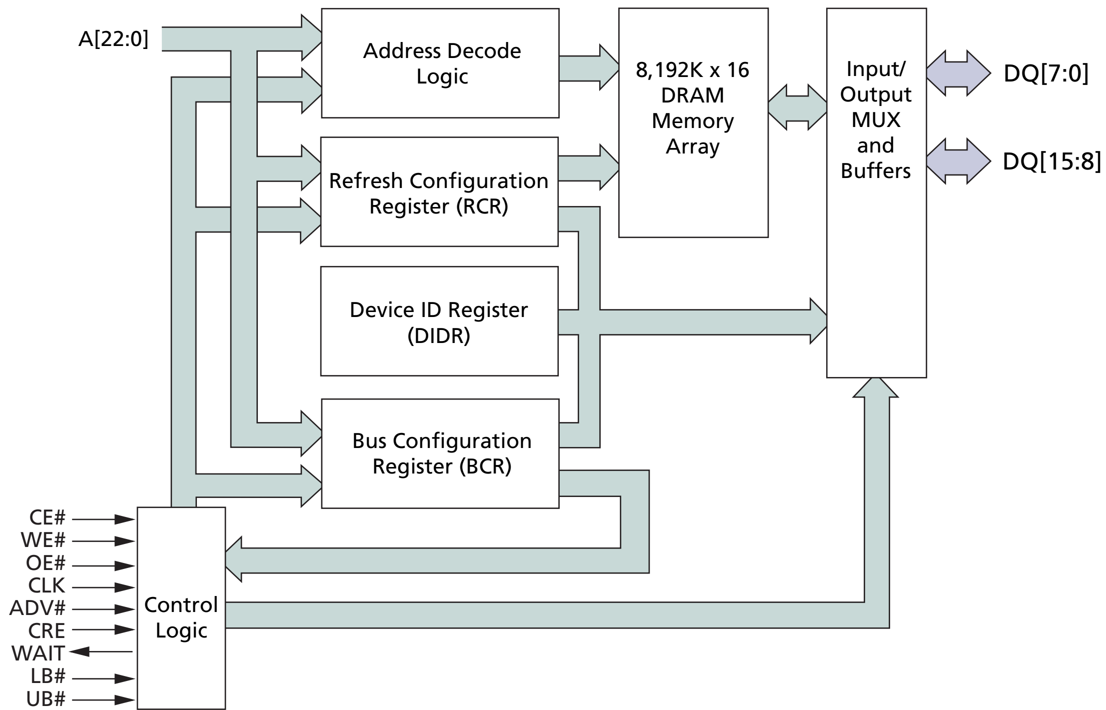
Figure 2: Functional Block Diagram – 8 Meg x 16



Notes: 1. Functional block diagrams illustrate simplified device operation. See ball descriptions (Table 1 on page 7), bus operations table (Table 2 on page 8), and timing diagrams for detailed information.

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Table 1: VFBGA Ball Descriptions
Note 1

VFBGA Assignment	Symbol	Type	Description
J4, E3, H6, G2, H1, D3, E4, F4, F3, G4, G3, H5, H4, H3, H2, D4, C4, C3, B4, B3, A5, A4, A3	A[22:0]	Input	Address inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR.
J2	CLK	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK is static LOW during asynchronous access READ and WRITE operations and during PAGE READ ACCESS operations.
J3	ADV#	Input	Address valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous READ and WRITE operations. ADV# can be held LOW during asynchronous READ and WRITE operations.
A6	CRE	Input	Control register enable: When CRE is HIGH, WRITE operations load the RCR or BCR, and READ operations access the RCR, BCR, or DIDR.
B5	CE#	Input	Chip enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or deep power-down mode.
A2	OE#	Input	Output enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
G5	WE#	Input	Write enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or to the memory array.
A1	LB#	Input	Lower byte enable. DQ[7:0]
B2	UB#	Input	Upper byte enable. DQ[15:8]
G1, F1, F2, E2, D2, C2, C1, B1, G6, F6, F5, E5, D5, C6, C5, B6	DQ[15:0]	Input/ Output	Data inputs/outputs.
J1	WAIT	Output	Wait: Provides data-valid feedback during burst READ and WRITE operations. The signal is gated by CE#. WAIT is used to arbitrate collisions between refresh and READ/WRITE operations. WAIT is also asserted at the end of a row unless wrapping within the burst length. WAIT is asserted and should be ignored during asynchronous and page mode operations. WAIT is High-Z when CE# is HIGH.
J5, J6	RFU	—	Reserved for future use.
D6	VCC	Supply	Device power supply: (1.7–1.95V) Power supply for device core operation.
E1	VCCQ	Supply	I/O power supply: (1.7–3.6V) Power supply for input/output buffers.
E6	VSS	Supply	VSS must be connected to ground.
D1	VSSQ	Supply	VSSQ must be connected to ground.

Notes: 1. The CLK and ADV# inputs can be tied to VSS if the device is always operating in asynchronous or page mode. WAIT will be asserted but should be ignored during asynchronous and page mode operations.

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Table 2: Bus Operations

Asynchronous Mode BCR[15] = 1	Power	CLK[1]	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT[2]	DQ[15:0][3]	Notes
Read	Active	L	L	L	L	H	L	L	Low-Z	Data-out	4
Write	Active	L	L	L	X	L	L	L	Low-Z	Data-in	4
Standby	Standby	L	X	H	X	X	L	X	High-Z	High-Z	5, 6
No operation	Idle	L	X	L	X	X	L	X	Low-Z	X	4, 6
Configuration register write	Active	L	L	L	H	L	H	X	Low-Z	High-Z	
Configuration register read	Active	L	L	L	L	H	H	L	Low-Z	Config. reg. out	
DPD	Deep power-down	L	X	H	X	X	X	X	High-Z	High-Z	7
Burst Mode BCR[15] = 0	**Power**	**CLK[1]**	**ADV#**	**CE#**	**OE#**	**WE#**	**CRE**	**LB#/ UB#**	**WAIT[2]**	**DQ[15:0][3]**	**Notes**
Async read	Active	L	L	L	L	H	L	L	Low-Z	Data-out	4
Async write	Active	L	L	L	X	L	L	L	Low-Z	Data-in	4
Standby	Standby	L	X	H	X	X	L	X	High-Z	High-Z	5, 6
No operation	Idle	L	X	L	X	X	L	X	Low-Z	X	4, 6
Initial burst read	Active		L	L	X	H	L	L	Low-Z	X	4, 8
Initial burst write	Active		L	L	H	L	L	X	Low-Z	X	4, 8
Burst continue	Active		H	L	X	X	X	L	Low-Z	Data-in or Data-out	4, 8
Burst suspend	Active	X	X	L	H	X	X	X	Low-Z	High-Z	4, 8
Configuration register write	Active		L	L	H	L	H	X	Low-Z	High-Z	8, 9
Configuration register read	Active		L	L	L	H	H	L	Low-Z	Config. reg. out	8, 9
DPD	Deep power-down	L	X	H	X	X	X	X	High-Z	High-Z	7

Notes:
1. CLK must be LOW during async read and async write modes; and to achieve standby power during standby and DPD modes. CLK must be static (HIGH or LOW) during burst suspend.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. V_{IN} = $V_{CC}Q$ or 0V; all device balls must be static (unswitched) in order to achieve standby current.
7. DPD is initiated when CE# transitions from LOW to HIGH after writing RCR[4] to 0. DPD is maintained until CE# transitions from HIGH to LOW.
8. Burst mode operation is initialized through the bus configuration register (BCR[15]).
9. Initial cycle. Following cycles are the same as BURST CONTINUE. CE# must stay LOW for the equivalent of a single-word burst (as indicated by WAIT).

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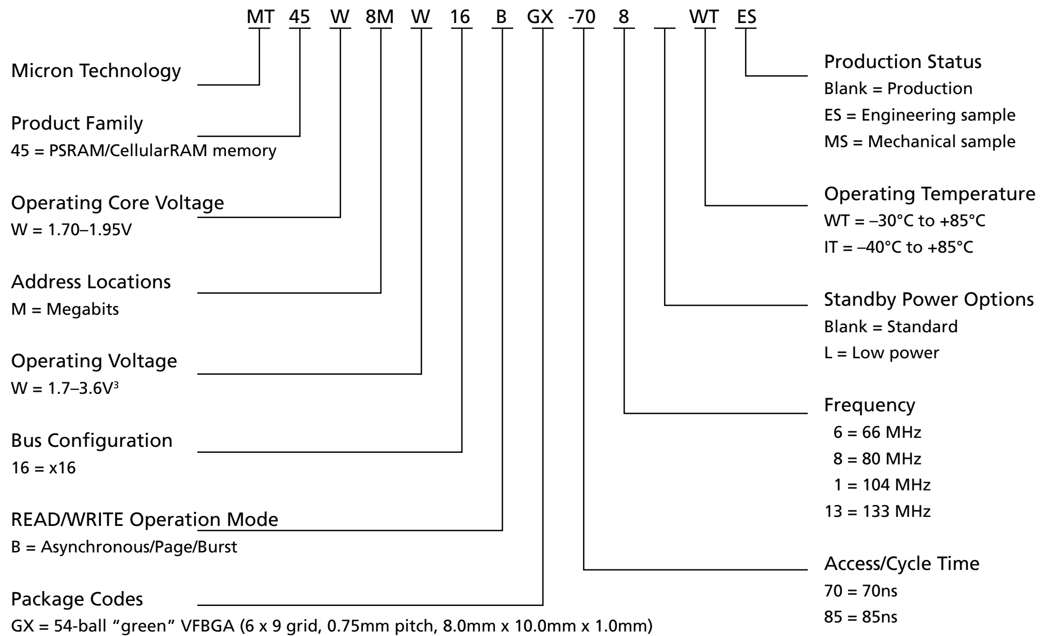
Part-Numbering Information

Micron CellularRAM devices are available in several different configurations and densities. (See Figure 3.)

Figure 3: Part Number Chart



Notes:
1. Valid part number combinations: After building the part number from the part numbering chart above, please go to the Micron Parametric Part Search Web site at http://www.micron.com/support/designsupport/tools/fbga/decoder to verify that the part number is offered and valid. If the device required is not on this list, please contact the factory.
2. Device marking: Due to the size of the package, the Micron standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at http://www.micron.com/support/designsupport/tools/fbga/decoder. To view the location of the abbreviated mark on the device, please refer to customer service note CSN-11, "Product Mark/Label," at http://www.micron.com/csn.
3. The 3.6V I/O exceeds the CellularRAM 1.5 Workgroup specification of 1.95V.

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Functional Description

In general, the MT45W8MW16BGX device is a high-density alternative to SRAM and pseudo-SRAM products, popular in low-power, portable applications.

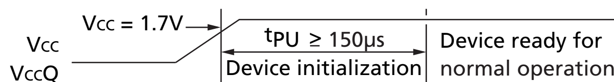
The MT45W8MW16BGX contains a 134,217,728-bit DRAM core, organized as 8,388,608 addresses by 16 bits. The device implements the same high-speed bus interface found on burst mode Flash products.

The CellularRAM bus interface supports both asynchronous and burst mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

Power-Up Initialization

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings. (See Figure 18 on page 24 and Figure 24 on page 31.) VCC and VCCQ must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150µs to complete its self-initialization process. During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

Figure 4: Power-Up Initialization Timing



Bus Operating Modes

The MT45W8MW16BGX CellularRAM product incorporates a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous, page mode, and burst mode read and write transfers. The specific interface supported is defined by the value loaded into the BCR. Page mode is controlled by the refresh configuration register (RCR[7]).

Asynchronous Mode

CellularRAM 1.5 products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control bus (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 5 on page 11) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (see Figure 6 on page 11) occur when CE#, WE#, and LB#/UB# are driven LOW. During asynchronous WRITE operations, the OE# level is a "Don't Care," and WE# will override OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). Asynchronous operations (page mode disabled) can either use the ADV# input to latch the address, or ADV# can be driven LOW during the entire READ/WRITE operation.

During asynchronous operation, the CLK input must be held static LOW. WAIT will be driven while the device is enabled and its state should be ignored. WE# LOW time must be limited to ^{t}CEM.

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