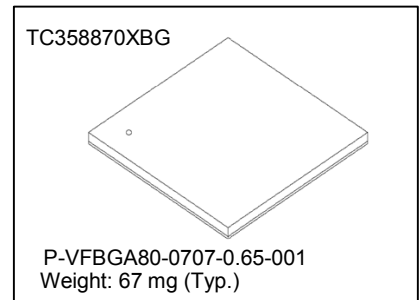


CMOS Digital Integrated Circuit Silicon Monolithic

# TC358870XBG

Mobile Peripheral Devices



## Overview

TC358870XBG, Ultra HD to DSI, bridge converts high resolution (higher than 4 Gbps) HDMI® stream to MIPI® DSI Tx video. It is a follow up device of TC358779XBG, without scalar functionality. The HDMI-RX runs at 297 MHz to carry up to 7.2 Gbps video stream. It requires dual link MIPI DSI Tx, 1 Gbps/data lane, to transmit out a maximum 7.2 Gbps video data.

The bridge chip is necessary for current and next generation Application Processors to drive a (dual) DSI link display by using its HDMI Tx output port.

## Features

### ● HDMI-RX Interface

- ◇ HDMI 1.4b
  - Video Formats Support (Up to 4K×2K / 30fps), maximum 24 bps (bit-per-pixel) no deep color support
    - RGB, YCbCr444: 24-bpp
    - YCbCr422: 24-bpp
  - Color Conversion
    - 4:2:2 to 4:4:4 is supported
    - 4:4:4: to 4:2:2 is supported
    - RGB888 to YCbCr (4:4:4 / 4:2:2) is supported
    - YCbCr (4:4:4 / 4:2:2) to RGB888/666 is supported
      - ◇ Note: for RGB666 (R=R[5:0],2'b00, G=G[5:0],2'b00, B=B[5:0],2'b00)
  - Maximum HDMI clock speed: 297 MHz
  - Audio Supports
    - Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
  - 3D Support
  - Support HDCP1.4 decryptions
  - EDID Support, Release A, Revision 1 (Feb 9, 2000)
    - First 128 byte (EDID 1.3 structure)
    - First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
    - Embedded 1K-byte SRAM (EDID\_SRAM)
- ◇ Does not support Audio Return Path and HDMI Ethernet Channels

### ● DSI TX Interface

- ◇ MIPI DSI compliant (Version 1.1 22 November 2011)
- ◇ Dual links DSI (DSI0 and DSI1), each link supports 4 data lanes @1 Gbps/ data lane
  - DSI0 carries the left half data of HDMI Rx video stream and DSI1 carries the right one at the default configuration.
  - Left or right data can be assigned/programmed to either DSI Tx link
  - The maximum length of each half is limited to

2048-pixel plus up to full length overlap, DSI0 data length could be different from that of DSI1's

- The maximum Hsync skew between DSI0 and DSI1 can be less than 10 ByteClk
- ◇ Single link DSI, maximum horizontal pixel width
  - 2558 pixels (24-bit per pixel)
  - 3411 pixels (16-bit per pixel)
- ◇ Supports video data formats
  - RGB666, RGB888, YCbCr444, YCbCr 422 16-bit and YCbCr 422 24-bit
  - YCbCr inputs can be converted into RGB before outputting

### ● I<sup>2</sup>C Interface

- ◇ Support for normal (100 kHz), fast mode (400 kHz) and ultrafast mode (2 MHz)
- ◇ Slave Mode
  - To be used by an external Master to configure all TC358870XBG internal registers, including EDID\_SRAM and panel control
  - Support 2 I<sup>2</sup>C Slave Addresses (0x0F & 0x1F) selected through boot-strap pin (INT)

### ● Audio Output Interface

- ◇ Up to four I2S data lines for supporting multi-Channel audio data (5.1 and 7.1)
- ◇ Maximum audio sample frequency supported is 192 kHz @8 CH
- ◇ Support 16, 18, 20 or 24-bit data (depend on HDMI input stream)
- ◇ Support Master Clock output only
- ◇ Support 32 bit-wide time-slot only
- ◇ Output Audio Over Sampling clock (256fs)
- ◇ Either I2S or TDM Audio interface available (pins are multiplexed)
- ◇ I2S Audio Interface
  - Support Left or Right-justify with MSB first
- ◇ TDM (Time Division Multiplexed) Audio Interface
  - Fixed to 8 channels (depend on HDMI input stream)

- ◇ Digital Audio Interface
  - Supports HBR audio stream split across 4 I2S lines if bandwidth higher than 12 MHz

- **InfraRed (IR)**

- ◇ Support NEC InfraRed protocol.

- **Power supply inputs**

- ◇ Core: 1.15V
- ◇ MIPI D-PHY: 1.2V
- ◇ I/O: 1.8V, 3.3V
- ◇ HDMI: 3.3V
- ◇ APLL: 3.3V

- **Power Consumption during typical operations**

- ◇ 1920×1080 @60 fps: 420 mW (Dual D-PHY link)
- ◇ 2560×1600 @60 fps: 504 mW (Dual D-PHY link)
- ◇ 3840×2160 @30 fps: 520 mW (Dual D-PHY link)

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1. MIPI D-PHY, "MIPI\_D-PHY\_specification\_v01-00-00, May 14, 2009"
2. MIPI DSI, "MIPI Alliance Specification for Display Serial Interface (DSI) Version 1.1 Revision 22 Nov 2011"
3. HDMI, "High-Definition Multimedia Interface Specification Version 1.4a March 4, 2010"
4. I<sup>2</sup>C bus specification, version 2.1, January 2000, Philips Semiconductor

# 1. Overview

TC358870XBG, Ultra HD to DSI, bridge converts high resolution (higher than 4 Gbps) HDMI® stream to MIPI® DSI Tx video. It is a follow up device of TC358779XBG without scalar/de-interlace capability. The HDMI-RX runs at 297 MHz to carry up to 7.2 Gbps video stream. It requires dual link MIPI DSI Tx, 1 Gbps/data lane, to transmit out a maximum 7.2 Gbps video data.

The bridge chip is necessary for current and next generation Application Processors to drive a (dual) DSI link display directly via its HDMI Tx output port.

TC358870XBG system view block diagrams is shown in Figure 1.1, respectively.

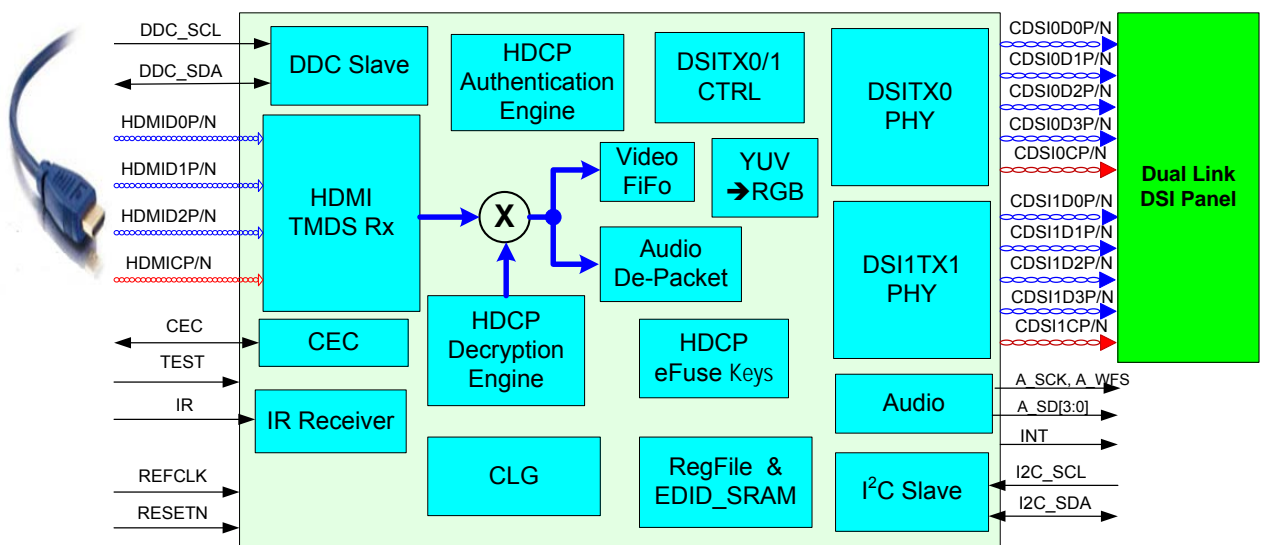


Figure 1.1 TC358870XBG System Overview



## 2. External Pins

TC358870XBG resides in BGA80 pin packages. The following table gives the signals of TC358870XBG and their function.

**Table 2.1 TC358870XBG Functional Signal List**

Group	Pin Name	Ball	I/O	Init (O)	Type (Note)	Function	Voltage Supply
SYSTEM (4)	RESETN	K8	I		Sch	System reset input (active low)	VDDIO18
	REFCLK	K9	I		Sch	Reference clock input (40 – 50 MHz)	VDDIO18
	TEST	G5	I		N	Internal test terminal (Always must be fixed low externally)	VDDIO18
	INT	J3	O	L	N	Interrupt Output signal (active high) *1	VDDIO18
CDSI TX0 (10)	CDSI0CP	F10	O	H	MIPI-PHY	MIPI-DSI0 clock positive	VDD12_MIPiO
	CDSI0CN	F9	O	H	MIPI-PHY	MIPI-DSI0 clock negative	VDD12_MIPiO
	CDSI0D0P	H10	O	H	MIPI-PHY	MIPI-DSI0 data 0 positive	VDD12_MIPiO
	CDSI0D0N	H9	O	H	MIPI-PHY	MIPI-DSI0 data 0 negative	VDD12_MIPiO
	CDSI0D1P	G10	O	H	MIPI-PHY	MIPI-DSI0 data 1 positive	VDD12_MIPiO
	CDSI0D1N	G9	O	H	MIPI-PHY	MIPI-DSI0 data 1 negative	VDD12_MIPiO
	CDSI0D2P	E10	O	H	MIPI-PHY	MIPI-DSI0 data 2 positive	VDD12_MIPiO
	CDSI0D2N	E9	O	H	MIPI-PHY	MIPI-DSI0 data 2 negative	VDD12_MIPiO
	CDSI0D3P	D10	O	H	MIPI-PHY	MIPI-DSI0 data 3 positive	VDD12_MIPiO
CDSI0D3N	D9	O	H	MIPI-PHY	MIPI-DSI0 data 3 negative	VDD12_MIPiO	
CDSI TX1 (10)	CDSI1CP	A7	O	H	MIPI-PHY	MIPI-DSI1 clock positive	VDD12_MIPiO
	CDSI1CN	B7	O	H	MIPI-PHY	MIPI-DSI1 clock negative	VDD12_MIPiO
	CDSI1D0P	A9	O	H	MIPI-PHY	MIPI-DSI1 data 0 positive	VDD12_MIPiO
	CDSI1D0N	B9	O	H	MIPI-PHY	MIPI-DSI1 data 0 negative	VDD12_MIPiO
	CDSI1D1P	A8	O	H	MIPI-PHY	MIPI-DSI1 data 1 positive	VDD12_MIPiO
	CDSI1D1N	B8	O	H	MIPI-PHY	MIPI-DSI1 data 1 negative	VDD12_MIPiO
	CDSI1D2P	A6	O	H	MIPI-PHY	MIPI-DSI1 data 2 positive	VDD12_MIPiO
	CDSI1D2N	B6	O	H	MIPI-PHY	MIPI-DSI1 data 2 negative	VDD12_MIPiO
HDMI-RX (9)	HDMICP	C1	I		HDMI-PHY	HDMI clock channel positive	VDD33_HDMI
	HDMICN	C2	I		HDMI-PHY	HDMI clock channel negative	VDD33_HDMI
	HDMID0P	D1	I		HDMI-PHY	HDMI data 0 channel positive	VDD33_HDMI
	HDMID0N	D2	I		HDMI-PHY	HDMI data 0 channel negative	VDD33_HDMI
	HDMID1P	E1	I		HDMI-PHY	HDMI data 1 channel positive	VDD33_HDMI
	HDMID1N	E2	I		HDMI-PHY	HDMI data 1 channel negative	VDD33_HDMI
	HDMID2P	F1	I		HDMI-PHY	HDMI data 2 channel positive	VDD33_HDMI
	HDMID2N	F2	I		HDMI-PHY	HDMI data 2 channel negative	VDD33_HDMI
	REXT	A1	I		HDMI-PHY	External reference resistor (Connect with 2kΩ to VDD33HDMI)	VDD33_HDMI
DDC (2)	DDC_SCL	A3	IO		Sch/5V/OD	DDC I <sup>2</sup> C slave clock	VDDIO33
	DDC_SDA	B3	IO		Sch/5V/OD	DDC I <sup>2</sup> C slave data	VDDIO33
CEC(1)	CEC	A2	IO		Sch/OD	CEC signal	VDDIO33
HPD(2)	HPDI	A4	I		5V	5V power input	VDDIO33
	HPDO	B4	O	L	N	Hot plug detect output	VDDIO33
Audio (7)	A_SCK	K7	O	L	N	I2S/TDM bit clock signal	VDDIO18
	A_WFS	K5	O	L	N	I2S word clock TDM frame sync signal	VDDIO18
	A_SD3	J5	O	L	N	I2S data signal bit3	VDDIO18
	A_SD2	J6	O	L	N	I2S data signal bit2	VDDIO18
	A_SD1	J8	O	L	N	I2S data signal bit1	VDDIO18
	A_SD0	J9	O	L	N	I2S data signal bit0 TDM data signal	VDDIO18
	A_OSCK	J4	O	L	N	Audio Over Sampling Clock	VDDIO18
IR(1)	IR	G6	I		N	InfraRed signal (Fix low externally, if not used)	VDDIO18
I2C(2)	I2C_SCL	K4	IO		Sch/OD	I <sup>2</sup> C slave clock	VDDIO18
	I2C_SDA	K3	IO		Sch/OD	I <sup>2</sup> C slave data	VDDIO18
Audio PLL	BIASDA	J1	O	L	PLL	Audio PLL BIAS signal	VDDIO33

Group	Pin Name	Ball	I/O	Init (O)	Type (Note)	Function	Voltage Supply
(4)						Connect to AVSS through 0.1 $\mu$ F when not used	
	DAOUT	J2	O	H	PLL	Audio PLL Clock Reference output clock Please leave open when not used	VDDIO33
	PCKIN	K1	I		PLL	Audio PLL Reference Input clock Connect to AVSS through 0.1 $\mu$ F when not used	VDDIO33
	PFIL	K2	O	L	PLL	Audio PLL Low Pass Filter signal Connect to AVSS through 0.1 $\mu$ F when not used	VDDIO33
POWER (10)	VDDC11	C10 K6	-		Power	1.1V Internal core power supply	-
	VDDIO18	J7	-		Power	1.8V IO power supply	-
	VDDIO33	H2	-		Power	3.3V IO power supply	-
	VDD33_HDMI	B1 G1	-		Power	HDMI Phy 3.3V power supply	-
	VDD11_HDMI	B2 G2	-		Power	HDMI Phy 1.1V power supply	-
	VDD12_MIPI0	J10	-		Power	MIPI DSI 1.2V power supply for link0	-
	VDD12_MIPI1	B10	-		Power	MIPI DSI 1.2V power supply for link1	-
GROUND (18)	VSS	A10 C9 D4 D5 D6 D7 E4 E5 E6 E7 F4 F5 F6 F7 G4 G7 H1 K10	-		-	Ground	-

Total 80 pins

Note: Descriptions mean below.

- N: Normal digital I/O
- Sch: Schmitt trigger input
- 5V: 5V tolerant input
- OD: Open drain
- \*1: Pull-Up to select 0x1F for I<sup>2</sup>C Slave address  
Pull-Down to select 0x0F for I<sup>2</sup>C Slave address

Please consult a technical support representative before board design to determine whether pull-up or pull-down with external resistors.

## 2.1. TC358870XBG 80-Pin Count Summary

Table 2.2 BGA80 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	-
CDSI TX0	10	-
CDSI TX1	10	-
HDMI-RX	9	-
DDC	2	-
CEC	1	-
Audio	7	-
I2C	2	-
IR	1	-
HPD	2	-
Audio PLL	4	-
POWER	10	IO, Core
GROUND	18	IO, Core, Analog
<b>TOTAL Pin Count</b>	<b>80</b>	Func 52 + (10+18)

## 2.2. Pin Layout

P-VFBGA80-0707-0.65

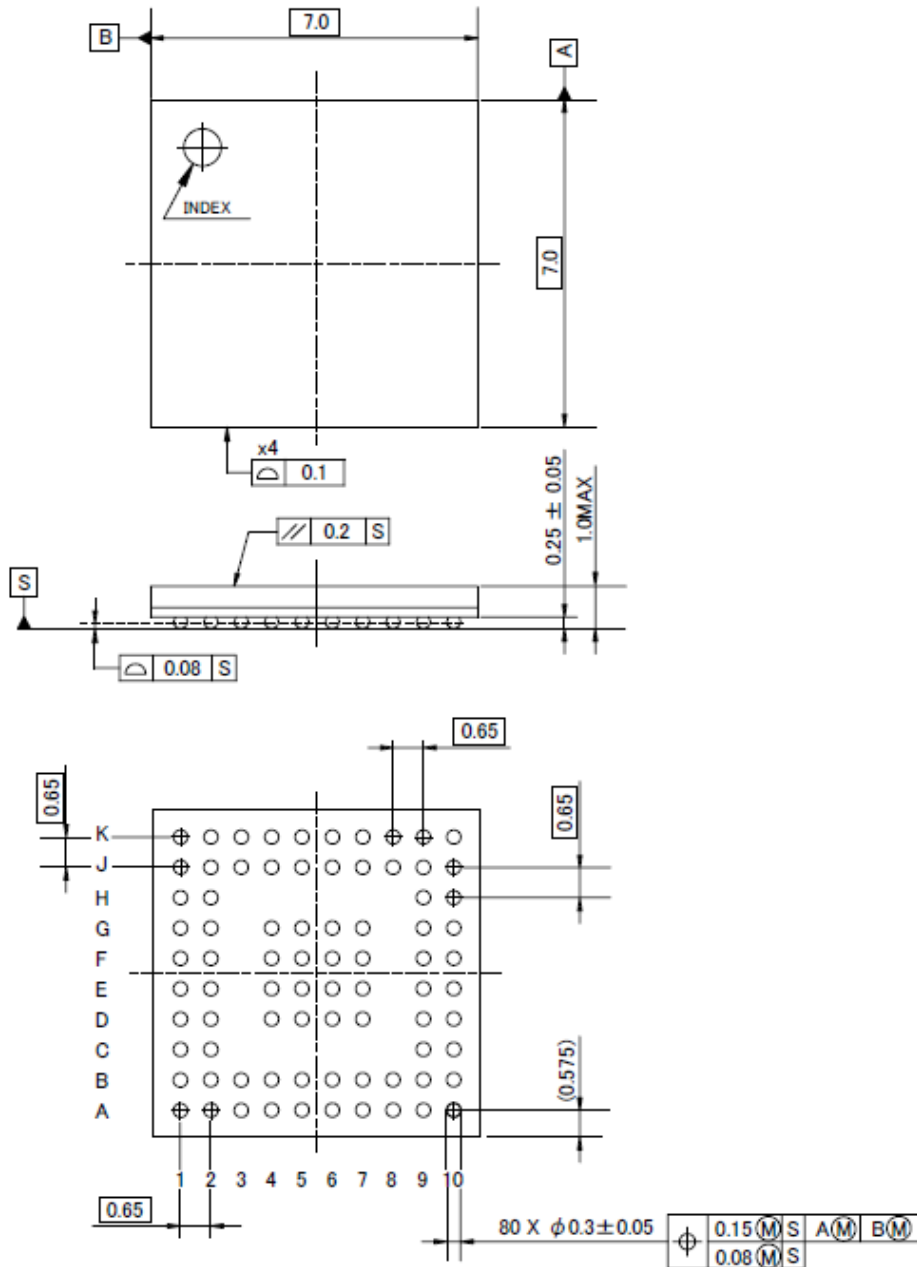
		Top view						CDSI1				
		1	2	3	4	5	6	7	8	9	10	
HDMI RX	A	A1 REXT	A2 CEC	A3 DDC_SCL	A4 HPDI	A5 CDSI1D3P	A6 CDSI1D2P	A7 CDSI1CP	A8 CDSI1D1P	A9 CDSI1D0P	A10 VSS	
	B	B1 VDD33_HDMI	B2 VDD11_HDMI	B3 DDC_SDA	B4 HPDO	B5 CDSI1D3N	B6 CDSI1D2N	B7 CDSI1CN	B8 CDSI1D1N	B9 CDSI1D0N	B10 VDD12_MIP1	
	C	C1 HDMICP	C2 HDMICN	C3 No ball	C4 No ball	C5 No ball	C6 No ball	C7 No ball	C8 No ball	C9 VSS	C10 VDDC11	
	D	D1 HDMID0P	D2 HDMID0N	D3 No ball	D4 VSS	D5 VSS	D6 VSS	D7 VSS	D8 No ball	D9 CDSI0D3N	D10 CDSI0D3P	
	E	E1 HDMID1P	E2 HDMID1N	E3 No ball	E4 VSS	E5 VSS	E6 VSS	E7 VSS	E8 No ball	E9 CDSI0D2N	E10 CDSI0D2P	
	F	F1 HDMID2P	F2 HDMID2N	F3 No ball	F4 VSS	F5 VSS	F6 VSS	F7 VSS	F8 No ball	F9 CDSI0CN	F10 CDSI0CP	
	G	G1 VDD33_HDMI	G2 VDD11_HDMI	G3 No ball	G4 VSS	G5 TEST	G6 IR	G7 VSS	G8 No ball	G9 CDSI0D1N	G10 CDSI0D1P	
	H	H1 VSS	H2 VDDIO33	H3 No ball	H4 No ball	H5 No ball	H6 No ball	H7 No ball	H8 No ball	H9 CDSI0D0N	H10 CDSI0D0P	
	APLL	J	J1 BIASDA	J2 DAOUT	J3 INT	J4 A_OSCK	J5 A_SD3	J6 A_SD2	J7 VDDIO18	J8 A_SD1	J9 A_SD0	J10 VDD12_MIP0
		K	K1 PCKIN	K2 PFIL	K3 I2C_SDA	K4 I2C_SCL	K5 A_WFS	K6 VDDC11	K7 A_SCK	K8 RESETN	K9 REFCLK	K10 VSS

Figure 2.1 TC358870XBG 80-Pin Layout (Top View)

### 3. Package

The 80-pin package for TC358870XBG is described in the figures below.

(Unit: mm)



Weight: 67mg (Typ.)

**Figure 3.1 TC358870XBG package (P-VFBGA80-0707-0.65-001)**

The mechanical dimension of BGA80 package is listed below.

**Table 3.1 Mechanical Dimension**

Package	Solder Ball Pitch	Solder Ball Height	Package Dimension	Package Height
80-Pin	0.65 mm	0.25 mm	7.0 × 7.0 mm <sup>2</sup>	1.0 mm

## 4. Electrical Characteristics

### 4.1. Absolute Maximum Ratings

VSS= 0V reference

Item	Symbol	Rating	Unit
Supply voltage (1.8V - Digital IO)	VDDIO18	-0.3 to +3.9	V
Supply voltage (3.3V - Digital IO)	VDDIO33	-0.3 to +3.9	V
Supply voltage (1.1V - Digital Core)	VDDC11	-0.3 to +1.8	V
Supply voltage (1.2V - MIPI DSI PHY)	VDD12_MIPI	-0.3 to +1.8	V
Supply voltage (3.3V - HDMIRX Phy)	VDD33_HDMI	-0.3 to +3.9	V
Supply voltage (1.1V - HDMIRX Phy)	VDD11_HDMI	-0.3 to +1.8	V
Input voltage (DSI IO)	V <sub>IN_DSI</sub>	-0.3 to VDD12_MIPI+0.3	V
Output voltage (DSI IO)	V <sub>OUT_DSI</sub>	-0.3 to VDD12_MIPI+0.3	V
Input voltage (Digital IO)	V <sub>IN_IO</sub>	-0.3 to VDDIO18+0.3 -0.3 to VDDIO33+0.3	V
Output voltage (Digital IO)	V <sub>OUT_IO</sub>	-0.3 to VDDIO18+0.3	V
Junction temperature	T <sub>j</sub>	125	°C
Storage temperature	T <sub>stg</sub>	-40 to +125	°C

### 4.2. Operating Condition

VSS= 0V reference

Item	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8V - Digital IO)	VDDIO18 <sup>note</sup>	1.65	1.8	1.95	V
Supply voltage (3.3V - Digital IO)	VDDIO33	3.0	3.3	3.6	V
Supply voltage (1.1V - Digital Core)	VDDC11	1.1	1.15	1.2	V
Supply voltage (3.3V - HDMIRX PHY)	VDD33_HDMI	3.135	3.3	3.465	V
Supply voltage (1.1V - HDMIRX PHY)	VDD11_HDMI	1.1	1.15	1.2	V
Supply voltage (1.2V - MIPI DSI PHY)	VDD12_MIPI0 VDD12_MIPI1	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	T <sub>a</sub>	-30	+25	+70	°C

Note: VDDIO18 can be used at 1.8V or 3.3V.

## 4.3. DC Electrical Specification

Standard IO

Item	Symbol	Min	Max	Unit
Input voltage, High level input <sup>Note1</sup>	V <sub>IH</sub>	0.70 VDDIO18 <sup>Note2</sup>	VDDIO18 <sup>Note2</sup>	V
		0.61 VDDIO18 <sup>Note3</sup>	VDDIO18 <sup>Note3</sup>	
		0.61 VDDIO33 <sup>Note4</sup>	VDDIO33 <sup>Note4</sup>	
Input voltage, Low level input <sup>Note1</sup>	V <sub>IL</sub>	0	0.30 VDDIO18 <sup>Note2</sup>	V
			0.25 VDDIO18 <sup>Note3</sup>	
			0.25 VDDIO33 <sup>Note4</sup>	
Input voltage High level CMOS Schmitt Trigger <sup>Note1</sup>	V <sub>IHS</sub>	0.70 VDDIO18 <sup>Note2</sup>	VDDIO18 <sup>Note2</sup>	V
		0.61 VDDIO18 <sup>Note3</sup>	VDDIO18 <sup>Note3</sup>	
		0.61 VDDIO33 <sup>Note4</sup>	VDDIO33 <sup>Note4</sup>	
Input voltage Low level CMOS Schmitt Trigger <sup>Note1</sup>	V <sub>ILS</sub>	0	0.30 VDDIO18 <sup>Note2</sup>	V
			0.25 VDDIO18 <sup>Note3</sup>	
			0.25 VDDIO33 <sup>Note4</sup>	
Output voltage High level <sup>Note1</sup>	V <sub>OH</sub>	VDDIO18-0.45 <sup>Note2</sup>	-	V
		VDDIO18-0.6 <sup>Note3</sup>		
		VDDIO33-0.6 <sup>Note4</sup>		
Output voltage Low level <sup>Note1</sup>	V <sub>OL</sub>	-	0.45 <sup>Note2</sup>	V
			0.4 <sup>Note3 Note4</sup>	
Input leak current, High level (Condition: VIN = +VDDIO, VDDIO = 3.6V)	I <sub>ILH1</sub>	-10	10	μA
Input leak current, Low level (Condition: VIN = 0V, VDDIO = 3.6V)	I <sub>ILL1</sub>	-10	10	μA

Note1: Each power source is operating within recommended operation condition.

Note2: For IOs related to VDDIO18 and operated at 1.8V range.

Note3: For IOs related to VDDIO18 and operated at 3.3V range.

Note4: For IOs related to VDDIO33.

HDMI DDC Slave IO (DDC\_SDA, DDC\_SCL terminal)

Item	Symbol	Min	Max	Unit
Input voltage, High level input	V <sub>IH</sub>	3.1	5.25	V
Input voltage, Low level input	V <sub>IL</sub>	0	1.7	V
Output voltage Low level(I <sub>OL</sub> =8mA)	V <sub>OL</sub>	-	0.4	V
Input leak current, High level (VIN=VDDIO33)	I <sub>IH</sub>	-10	10	μA
Input leak current, Low level(VIN=VSS)	I <sub>IL</sub>	-10	10	μA

HDMI CEC IO (CEC terminal)

Item	Symbol	Min	Max	Unit
Input voltage, High level input	V <sub>IH</sub>	2	VDDIO33	V
Input voltage, Low level input	V <sub>IL</sub>	0	0.8	V
Output voltage Low level(I <sub>OL</sub> =8mA)	V <sub>OL</sub>	-	0.4	V
Input leak current, High level(VIN=VDDIO33)	I <sub>IH</sub>	-10	10	μA
Input leak current, Low level(VIN=VSS)	I <sub>IL</sub>	-10	10	μA

I<sup>2</sup>C IO (I2C\_SDA, I2C\_SCL terminal)

Item	Symbol	Min	Max	Unit
Input voltage, High level input	V <sub>IH</sub>	0.7VDDIO18	VDDIO18	V
Input voltage, Low level input	V <sub>IL</sub>	0	0.3VDDIO18	V
Output voltage Low level (VDDIO18 used at 1.8V, I <sub>OL</sub> =3mA)	V <sub>OL</sub>	-	0.2VDDIO18	V
Output voltage Low level (VDDIO18 used at 3.3V, I <sub>OL</sub> =3mA)		-	0.4	V

## 5. External Circuit Suggestion

### 5.1. I<sup>2</sup>C Slave address definition

INT terminal is multiplexed with configuring function of I<sup>2</sup>C Slave address. During **RESETN** asserted, **INT** becomes input and detects the polarity. After **RESETN** deasserted it becomes **INT** function (output) automatically. Pull up or pull down this terminal by 10kohm resistor externally.

If pulled up, then I<sup>2</sup>C Slave address becomes 0x1F

If pulled down then I<sup>2</sup>C Slave address becomes 0x0F

### 5.2. HDMI

**DDC\_SDA** and **DDC\_SCL** are pulled up to +5V power line and +5V power line is also pulled down for **DDC\_SDA** and **DDC\_SDL** to be fixed low when +5V power is disabled.

Below figure illustrates example DDC interface connections.

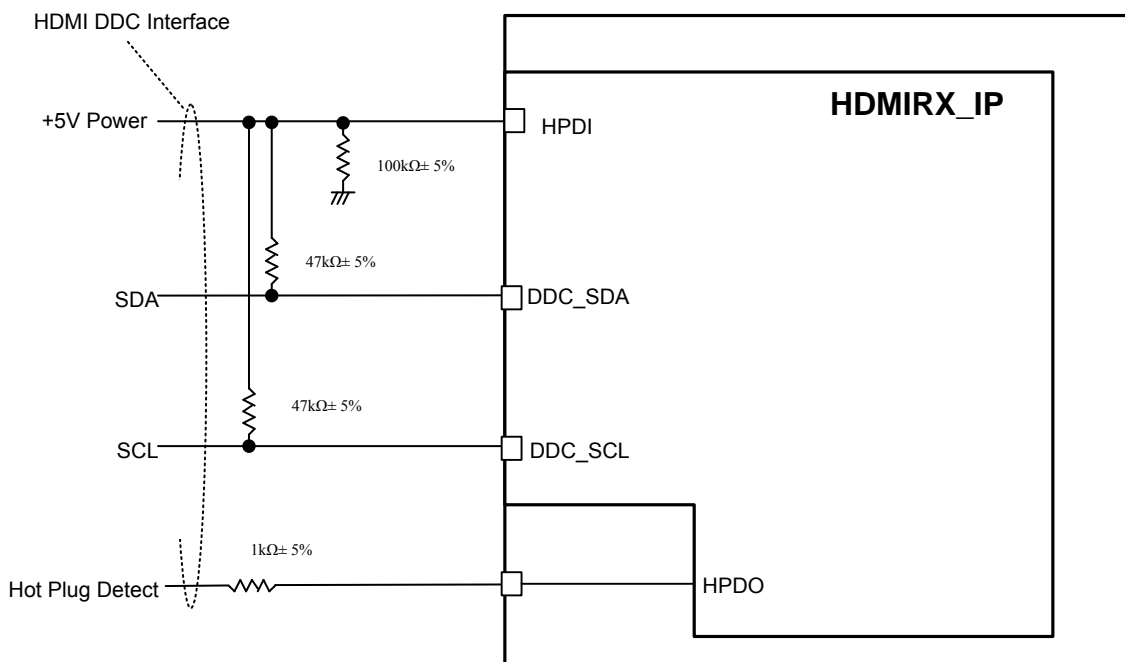


Figure 5.1 Example of DDC I/F Connection



The automatic adjustment function of terminus resistance is attached to HDMI-Rx.  
Therefore, connect  $2k\Omega \pm 1\%$  of reference resistance between **VDD33\_HDMI** and **REXT**.

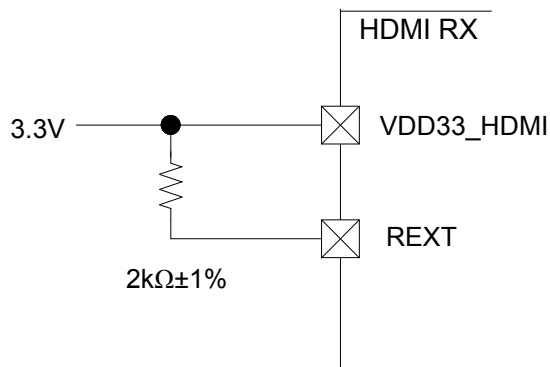


Figure 5.2 Connection of REXT resistance

### 5.3. Audio PLL

The Audio PLL external terminal connections used in the Audio clock generation are shown in the Figure below.  
In **DAOUT** output (PLL input), a low pass filter is installed in the LSI external area.  
In addition, a low pass filter for cutting unnecessary components in phase comparator output in the PLL is also installed in the LSI external area.

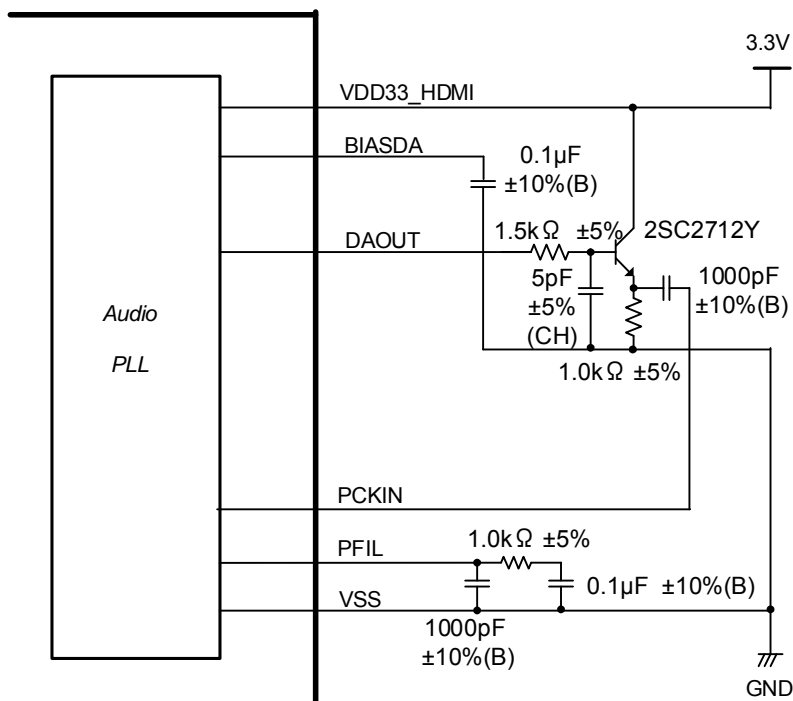


Figure 5.3 Audio Clock External LPF circuit block diagram

### 5.4. Suggestion of Power supply circuit

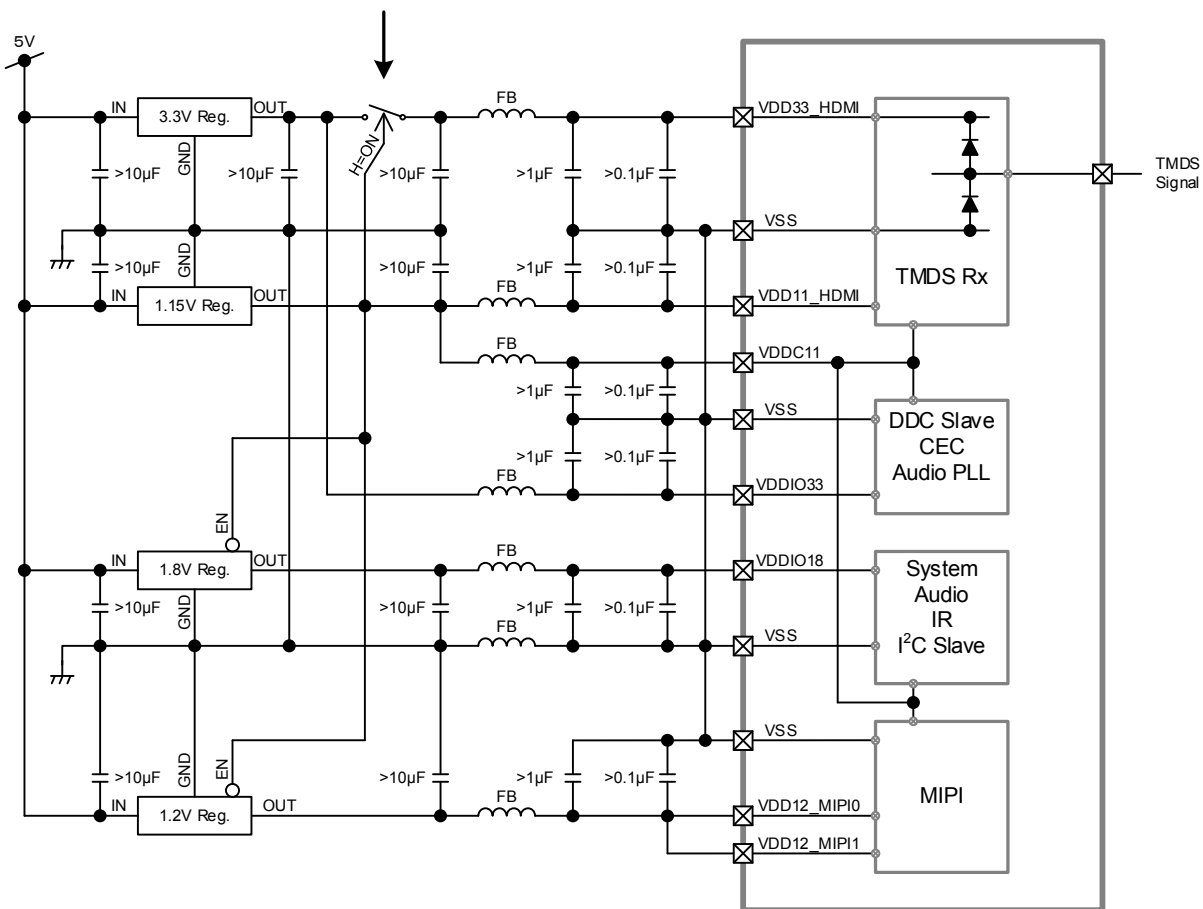
Since the ESD protection diode is attached to the TMDS input pin between a power supply/GND, current may flow backwards HDMI-Rx from source apparatus at the time of power supply OFF.

And also VDD33\_HDMI power supply should be isolated from another 3.3V power supplies because this backward current also damages them. Below figure is recommend attaching a back flow prevention circuit.

#### Case (1) External switch circuit

Attach the adverse current prevention switch from a TMDS differential signal.

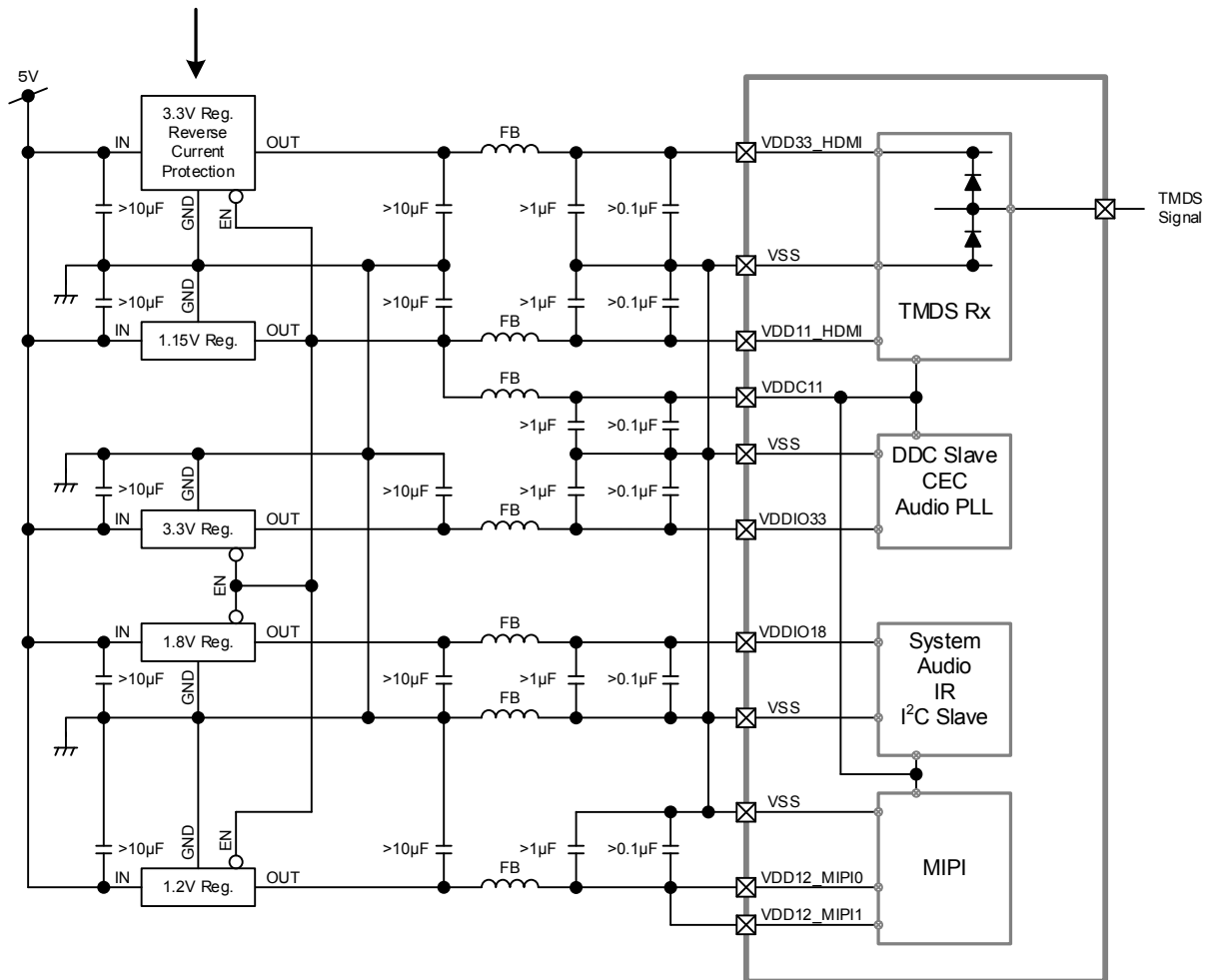
Since reverse current also gives damage to VDDIO33, this switch shall separate VDD33\_HDMI and VDDIO33.



All TC358870 VSSs should be separated at AC level from regulators' VSS with FB(ferrite bead) or another method to attenuate EMI.

**Figure 5.4 Suggestion of power supply circuit with external switch**

Case (2) Regulator with reverse current protection  
 Apply a current protection regulator to VDD33\_HDMI.



All TC358870 VSSs should be separated at AC level from regulators' VSS with FB(ferrite bead) or another method to attenuate EMI.

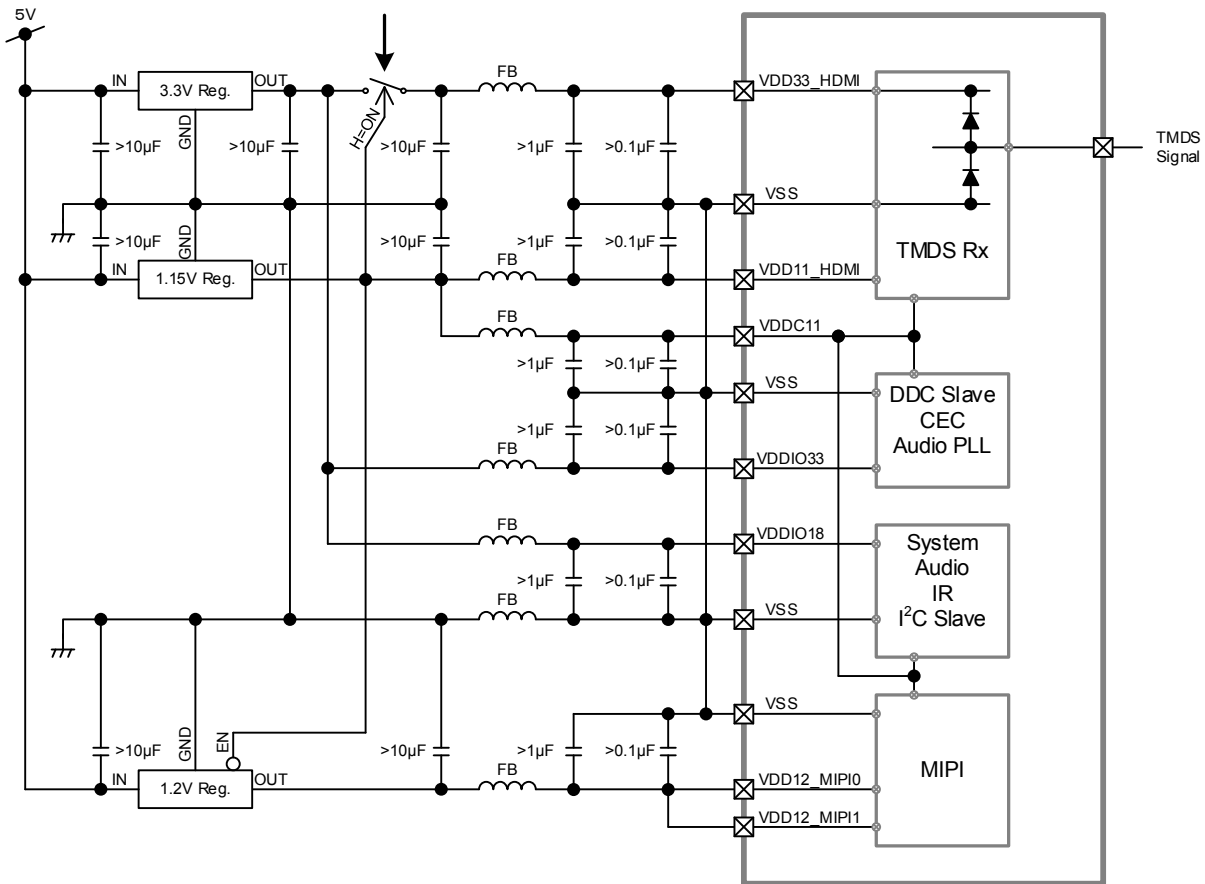
**Figure 5.5 Suggestion of power supply circuit with current protection regulator**

Case (3) Use of VDDIO18 at 3.3V range

If VDDIO is applied at 3.3V range, Common regulation is available among VDD33\_HDMI, VDIO33 and VDDIO18.

Attach the adverse current prevention switch from a TMDS differential signal.

Since reverse current also gives damage to VDDIO33 and VDDIO18, this switch shall separate VDD33\_HDMI and VDDIO33/VDDIO18.



All TC358870 VSSs should be separated at AC level from regulators' VSS with FB(ferrite bead) or another method to attenuate EMI.

Figure 5.6 Suggestion of power supply circuit at VDDIO18 = 3.3V

## 6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2014-08-01	New
1.1	2014-09-18	Remove registers 0x5008 and 0x5088 which are not used Remove Supply Noise Voltage, $V_{SN}$ , from Operation Condition table in section 8.2 Typo fixed 0x04_10 => 0x8410 Add more descriptions for 0x025C, 0x026C, NCO_48F, NCO_44F Remove "address 0x85_0F" and adding note
1.521	2015-12-18	Typo Init(O) DAOUT pin in External Pins
1.512	2016-04-01	• Modified the weight of TC358870XBG's package by rounding up digits after the decimal point to form an integer.

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