1Gb DDR2 SDRAM

H5PS1G63JFR-xxC
H5PS1G63JFR-xxI
H5PS1G63JFR-xxL
H5PS1G63JFR-xxJ

Ordering Information

Part No.	Configuration	Power Consumption	Operation Temp	Package
H5PS1G63JFR-xx*C	64Mx16	Normal Consumption	Commercial	84 Ball fBGA
H5PS1G63JFR-xx*I		Normal Consumption	Industrial	
H5PS1G63JFR-xx*L		Low Power Consumption (IDD6 Only)	Commercial	
H5PS1G63JFR-xx*J		Low Power Consumption (IDD6 Only)	Industrial	

Note:

-XX* is the speed bin, refer to the Operating Frequency table for complete part number.
-xxP and xxQ are the low current bin, refer to the IDD specification table.
- SK hynix Halogen-free products are compliant to RoHS.
SK hynix supports Lead & Halogen free parts for each speed grade with same specification, except Lead free materials.
We'll add "R" character after "F" for Lead & Halogen free products

Operating Frequency

Grade	tCK(ns)	CL	tRCD	tRP	Unit
E3	5	3	3	3	Clk
C4	3.75	4	4	4	Clk
Y5	3	5	5	5	Clk
S6	2.5	6	6	6	Clk
S5	2.5	5	5	5	Clk
G7	1.875	7	7	7	Clk

Note:

-G7 is a special speed product used in electronic engineering for high speed storage of the working data of a consumer digital electronic device.
- x16 product only

1.2 Pin Configuration & Address Table

64Mx16 DDR2 PIN CONFIGURATION(Top view: see balls through package)

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	$\overline{\text{UDQS}}$	VDDQ
DQ14	VSSQ	UDM	B	UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ	C	VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11	D	DQ10	VSSQ	DQ13
VDD	NC	VSS	E	VSSQ	$\overline{\text{LDQS}}$	VDDQ
DQ6	VSSQ	LDM	F	LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	G	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	H	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	J	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	K	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
BA2	BA0	BA1	L	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10/AP	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	NC	R	NC	NC	

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 1.0 V ~ 2.3 V	V	1
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
VDDL	Voltage on VDDL pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2
I_I	Input leakage current; any input 0V VIN VDD; all other balls not under test = 0V)	-2 uA ~ 2 uA	uA	
I_{OZ}	Output leakage current; 0V VOUT VDDQ; DQ and ODT disabled	-5 uA ~ 5 uA	uA	

Note:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range	85 to 95	°C	1,4
	Industrial Temperature Range	-40 to 95	°C	1,3,4

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	1,2
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1,2
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3,4
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	5

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IH}(dc)$	dc input logic HIGH	VREF + 0.125	VDDQ + 0.3	V	
$V_{IL}(dc)$	dc input logic LOW	- 0.3	VREF - 0.125	V	

3.2.2 Input AC Logic Level

Symbol	Parameter	DDR2 400,533		DDR2 667,800		Units	Notes
		Min.	Max.	Min.	Max.		
V_{IH} (ac)	ac input logic HIGH	VREF + 0.250	VDDQ+Vpeak	VREF + 0.200	VDDQ+Vpeak	V	
V_{IL} (ac)	ac input logic LOW	VSSQ-Vpeak	VREF - 0.250	VSSQ-Vpeak	VREF - 0.200	V	

Symbol	Parameter	DDR2 1066		Units	Notes
		Min.	Max.		
V_{IH} (ac)	ac input logic HIGH	VREF + 0.200	VDDQ+Vpeak	V	
V_{IL} (ac)	ac input logic LOW	VSSQ-Vpeak	VREF - 0.200	V	

3.2.3 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Symbol		DDR2 667	DDR2 800	DDR2 1066	Units
		x16	x16	x16	
IDD0		65.0	70.0	75.0	mA
IDD1		70.0	75.0	80.0	mA
IDD2P		10.0	10.0	10.0	mA
IDD2Q		23.0	24.0	25.0	mA
IDD2N		27.0	29.0	29.0	mA
IDD3P	F	15	15	15	mA
	S	10	10	10	mA
IDD3N		34.0	37.0	40.0	mA
IDD4W		100.0	105.0	125.0	mA
IDD4R		95.0	105.0	140.0	mA
IDD5		125.0	130.0	135.0	mA
IDD6	Normal	10.0	10.0	10.0	mA
	Low power	5.0	5.0	5.0	mA
IDD7		265.0	280.0	295.0	mA

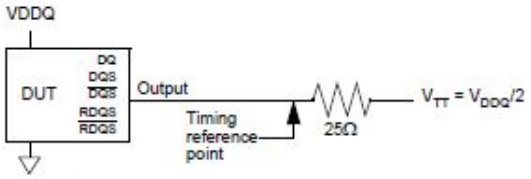
Note : Product list

Part No.	Configuration	Power Consumption	Operation Temp	Package
H5PS1G63JFR-xx*C	64Mx16	Normal Consumption	Commercial	84 Ball fBGA
H5PS1G63JFR-xx*I		Normal Consumption	Industrial	
H5PS1G63JFR-xx*L		Low Power Consumption (IDD6 Only)	Commercial	
H5PS1G63JFR-xx*J		Low Power Consumption (IDD6 Only)	Industrial	

Symbol	Conditions		Units
IDD0	**Operating one bank active-precharge current;** $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RAS}$ min(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;Address bus inputs are SWITCHING;Data bus inputs are SWITCHING		mA
IDD1	**Operating one bank active-read-precharge current;** IOUT = 0mA;BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC}$ (IDD), $t_{RAS} = t_{RAS}$min(IDD), $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA
IDD2P	**Precharge power-down current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA
IDD2Q	**Precharge quiet standby current;**All banks idle; $t_{CK} = t_{CK(IDD)}$;CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA
IDD2N	**Precharge standby current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD3P	**Active power-down current;** All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MR(12) = 0	mA
		Slow PDN Exit MR(12) = 1	mA
IDD3N	**Active standby current;** All banks open; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD4W	**Operating burst write current;** All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD4R	**Operating burst read current;** All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA
IDD5B	**Burst refresh current;** $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA
IDD6	**Self refresh current;** CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		mA
IDD7	**Operating bank interleave read current;** All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $t_{RCD(IDD)}$-1*$t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RRD} = t_{RRD(IDD)}$, $t_{RCD} = 1*t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following page for detailed timing conditions		mA

1. DDR2 SDRAM AC timing reference load

The following figure represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).



AC Timing Reference Load

The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. $\overline{DQS}$) signal.

2. Slew Rate Measurement Levels

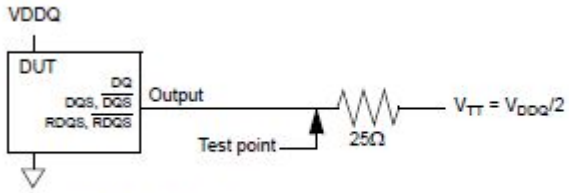
a. Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals. For differential signals (e.g. DQS - $\overline{DQS}$) output slew rate is measured between DQS - $\overline{DQS}$ = -500 mV and DQS - $\overline{DQS}$ = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

b. Input slew rate for single ended signals is measured from dc-level to ac-level: from VREF - 125 mV to VREF + 250 mV for rising edges and from VREF + 125 mV and VREF - 250 mV for falling edges. For differential signals (e.g. CK - $\overline{CK}$) slew rate for rising edges is measured from CK - $\overline{CK}$ = -250 mV to CK - $\overline{CK}$ = +500 mV (+250mV to -500 mV for falling edges).

c. VID is the magnitude of the difference between the input voltage on CK and the input voltage on $\overline{CK}$, or between DQS and $\overline{DQS}$ for differential strobe.

3. DDR2 SDRAM output slew rate test load

Output slew rate is characterized under the test conditions as shown below.



Slew Rate Test Load

4. Differential data strobe

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMR "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMR, the complementary pin, $\overline{DQS}$, must be tied externally to VSS through a 20 Ω to 10 KΩ resistor to insure proper operation.

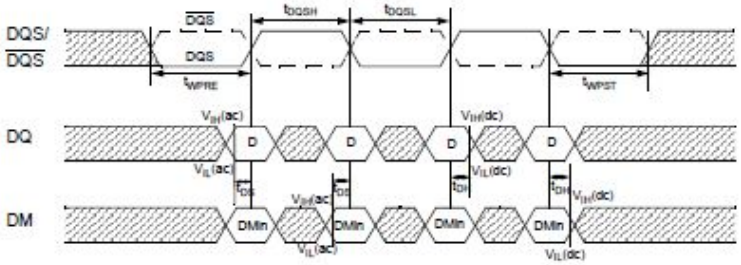


Figure -- Data input (write) timing

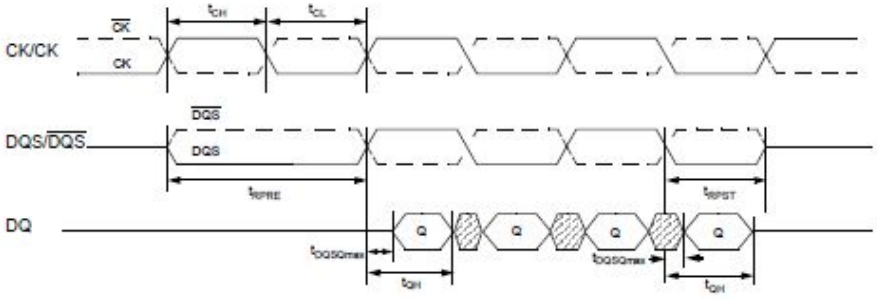


Figure -- Data output (read) timing

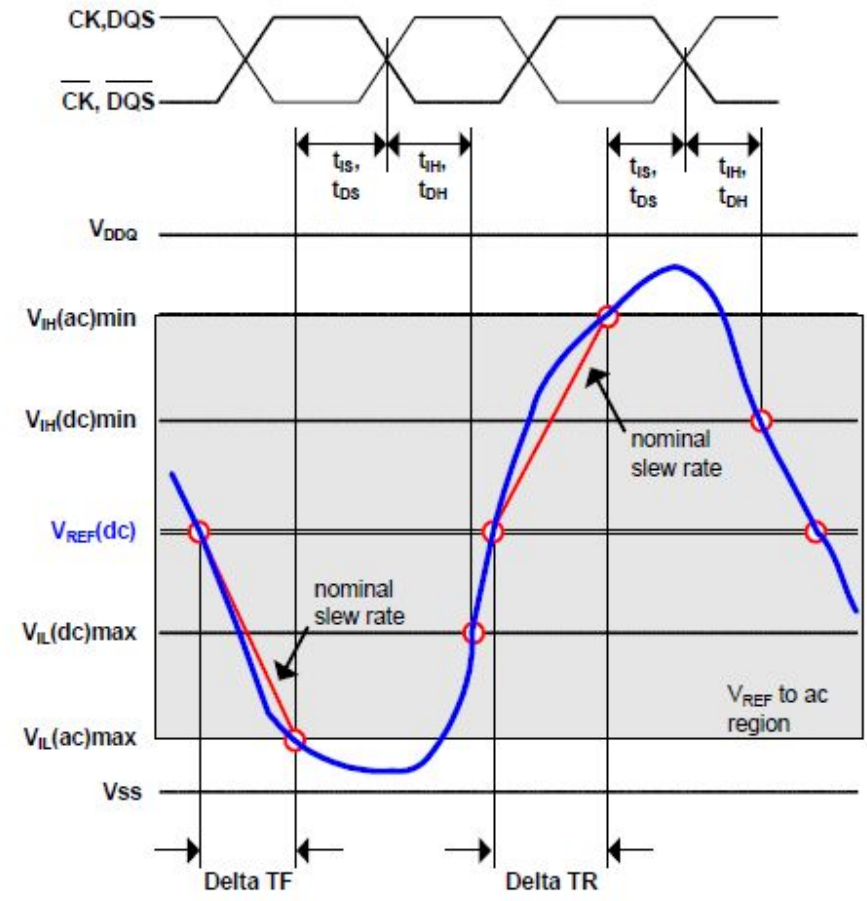
5. AC timings are for linear signal transitions. See System Derating for other signal transitions.

6. All voltages referenced to VSS.

7. These parameters guarantee device behavior, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

8. Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

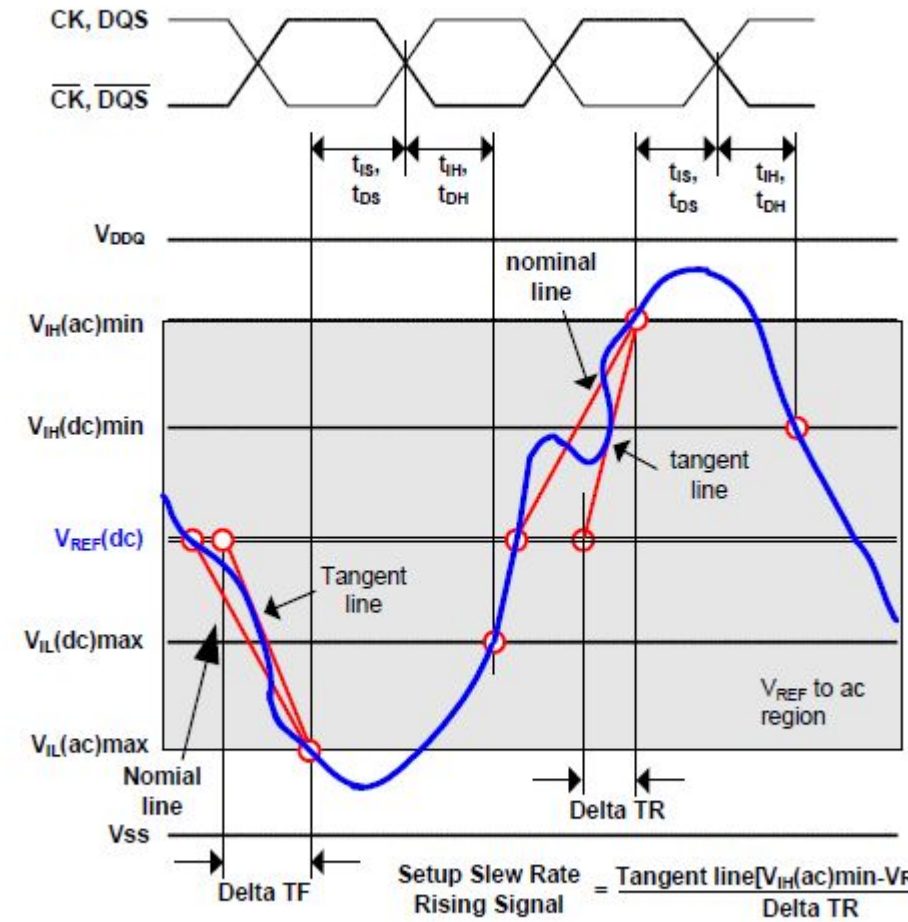
Fig. a. Illustration of nominal slew rate for tIS,tDS



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF}(dc) - V_{IL}(ac)max}{\text{Delta TF}}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH}(ac)min - V_{REF}(dc)}{\text{Delta TR}}$$

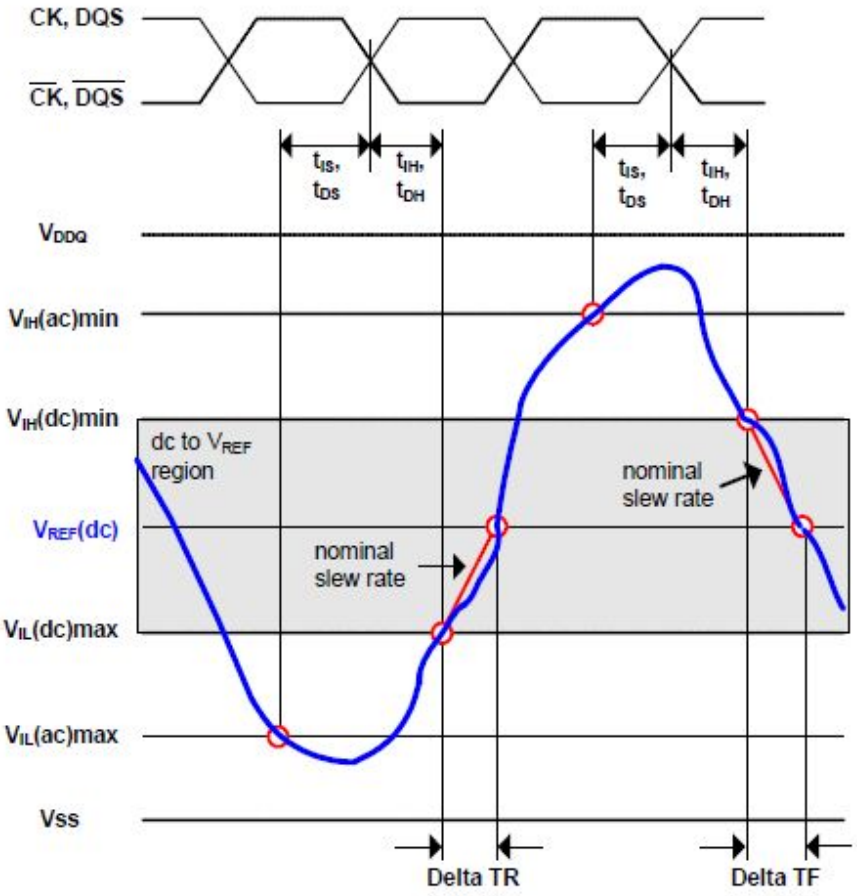
Fig. b. Illustration of tangent line for tIS,tDS



$$\text{Setup Slew Rate Rising Signal} = \frac{\text{Tangent line}[V_{IH}(ac)\text{min} - V_{REF}(dc)]}{\text{Delta TR}}$$

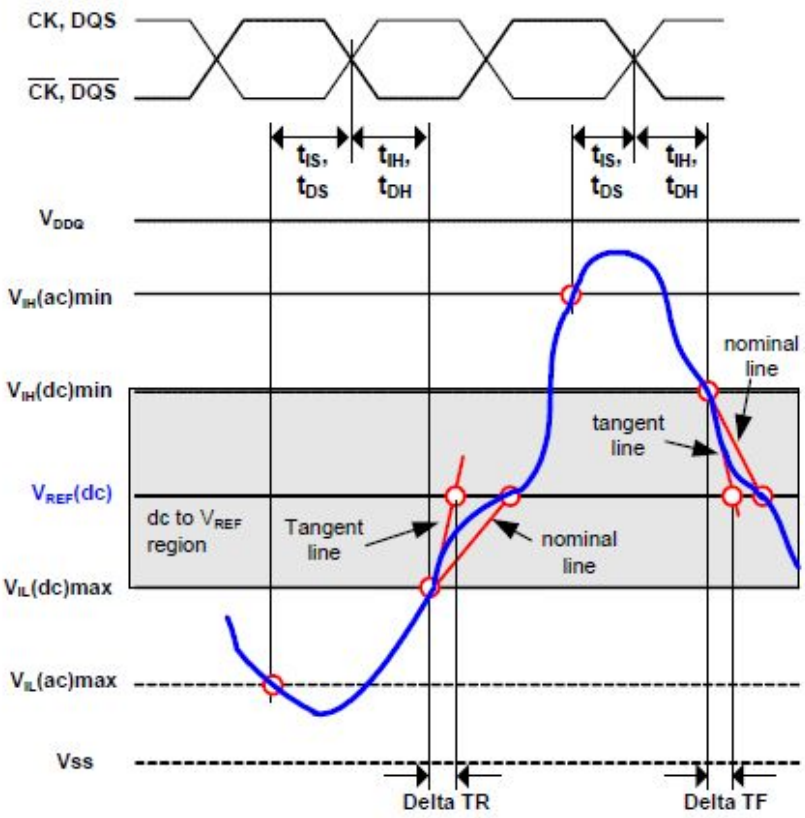
$$\text{Setup Slew Rate Falling Signal} = \frac{\text{Tangent line}[V_{REF}(dc) - V_{IL}(ac)\text{max}]}{\text{Delta TF}}$$

Fig. c. Illustration of nominal line for tIH, tDH



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF}(dc) - V_{IL}(dc)max}{\text{Delta TR}} \qquad \text{Hold Slew Rate Falling Signal} = \frac{V_{IH}(dc)min - V_{REF}(dc)}{\text{Delta TF}}$$

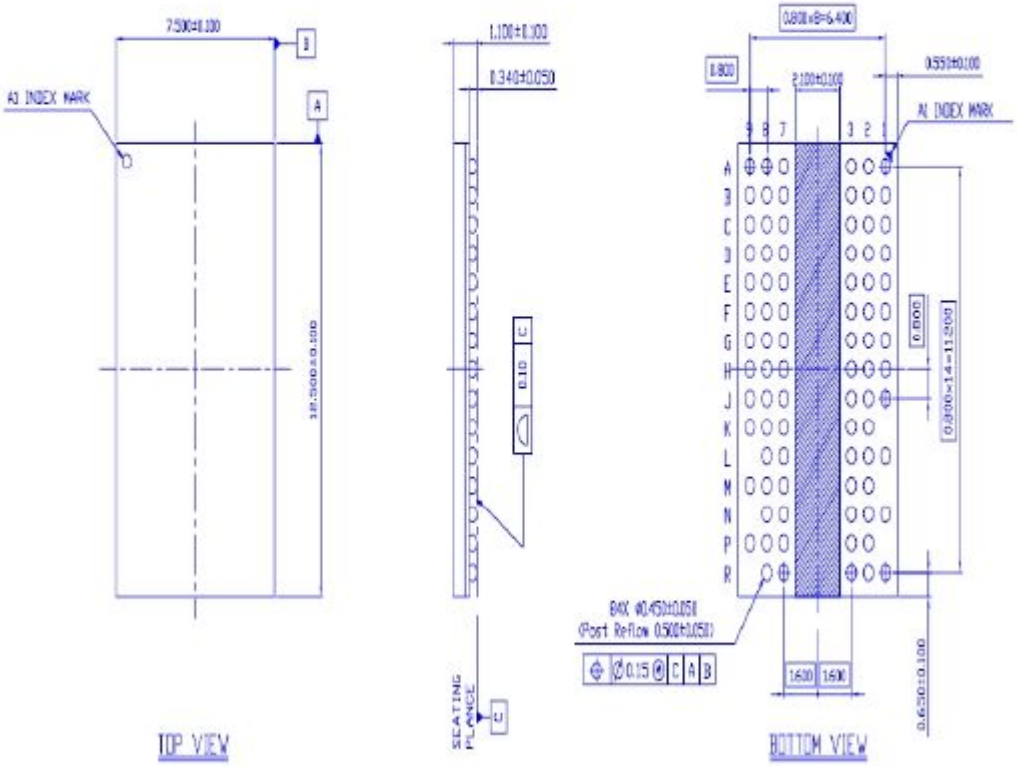
Fig. d. Illustration of tangent line for tIH, tDH

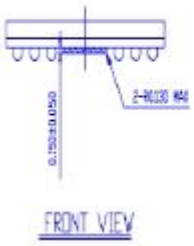


$$\text{Hold Slew Rate Rising Signal} = \frac{\text{Tangent line}[V_{REF}(dc) - V_{IL}(ac)max]}{\text{Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{Tangent line}[V_{IH}(ac)min - V_{REF}(dc)]}{\text{Delta TF}}$$

84Ball Fine Pitch Ball Grid Array Outline





SK-HYNIX 全新原装现货 深圳市廊宇达科技有限公司优势供应

热线：0755-83251635 QQ：1801896095